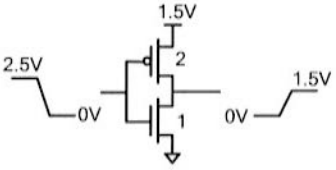
S-87.3182 Digital microelectronics I: System level electric design (5 cr)
17.12.2012. Please write clearly. Voit vastata myös **suomeksi**

1) a) Implement the logic function $Out = \overline{A \oplus B \oplus C}$, (where $\oplus$ is XOR) with a static CMOS gate. You can assume that both the true and complementary versions of input are available (e.g. A and $\overline{A}$ are available simultaneously). (5p)

b) Lowering VDD can be the best method to save power. If the inverter on the right was compared to an inverter with a supply voltage of 2.5V. What is the logical effort of this inverter for the rising transition at the output? (If you do not remember the equations, explain how the logical effort changes.) (5p)

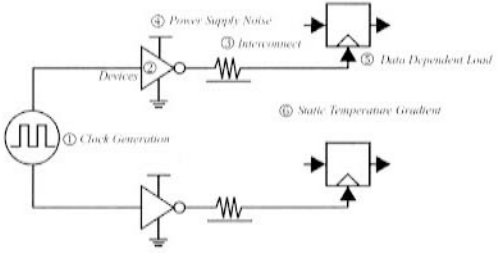


2) a) For a latch or flip-flop, explain the terms t_s, t_h, t_a, t_{dCQ}, and t_{cCQ}. (a diagram would be helpful here) (3p)

b) Draw a transistor-level schematic of a MUX-based latch and use this diagram to explain the physical causes of t_a, t_h, and t_{dCQ}. (4p)

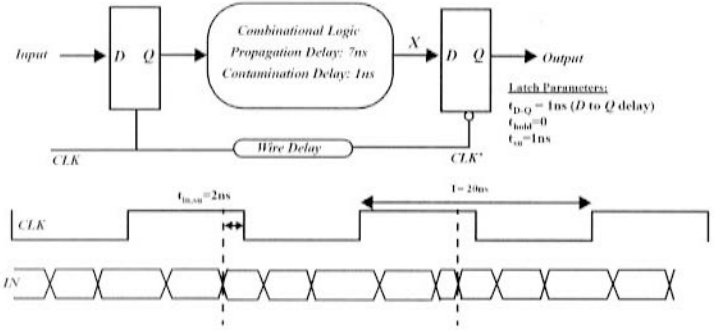
c) Explain how this latch can enter a metastable state? (3p)

3) A balanced clock distribution scheme is shown on the right. Explain each source of variation and identify whether it contributes to skew or jitter. (4p)

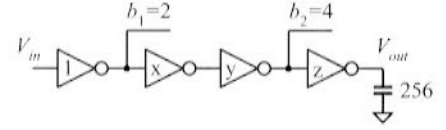


TURN OVER =>

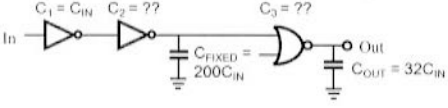
b) Consider the following latch based pipeline circuit shown below. Assume that the input, IN, is valid (i.e., set up) 2ns before the falling edge of CLK and is held till the falling edge of CLK (there is no guarantee on the value of IN at other times). Determine the maximum positive and negative skew on CLK' for correct functionality. (You can assume that $t_{C\text{-}Q}$ is also 1ns.) (6p)



4) a) Consider the circuit below. Determine scaling factors x, y, z to minimize the delay. The output capacitance is 256 times the input capacitance. (5p)



b) Consider the logic chain shown below, where C_{IN} = 3fF. The two inverters buffer a signal which goes across chip to another logic block. The wire that the two inverters drive has a fixed (i.e., independent of sizing) capacitance of $C_{FIXED} = 200C_{IN}$. This fixed capacitance is sometimes called a side-load (ignore any resistance of the side-load).
Derive the equation for the delay of this chain in terms of the input capacitances of the three gates (C_1, C_2, C_3), the capacitances C_{FIXED} and C_L, γ, and t_{inv}. (5p)



Extra. Leave feedback about the course on the exam paper. Especially Enrico is interested in his performance. (1p)