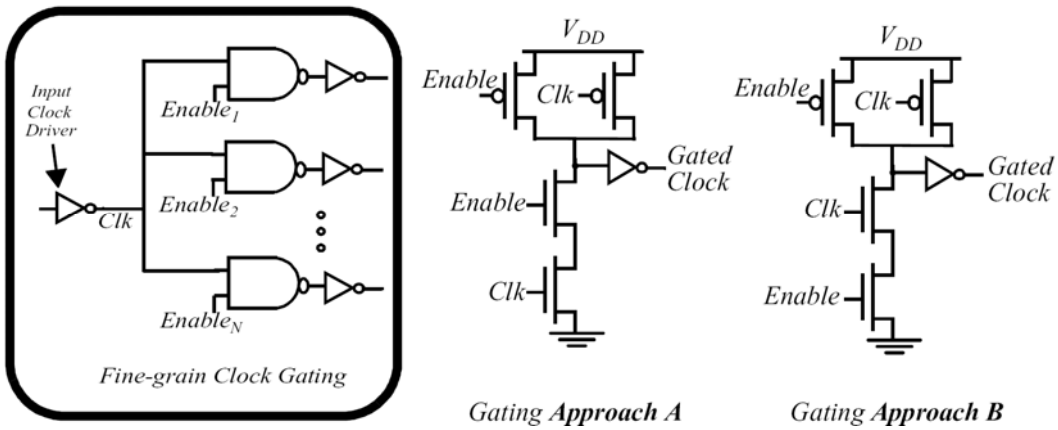
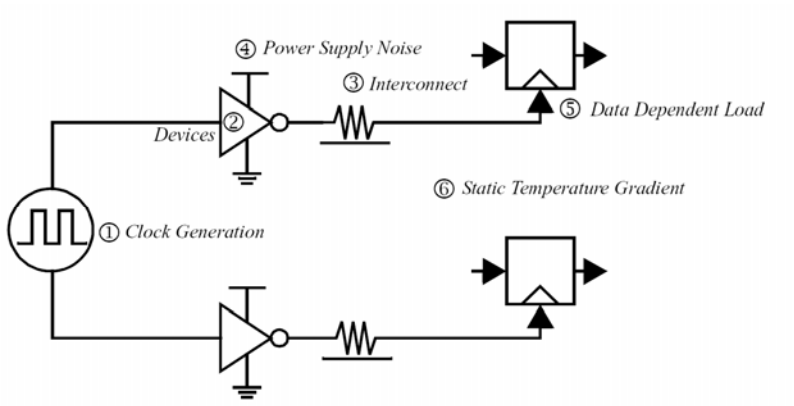
S-87.3182 Digital microelectronics I: System level electric design (5 cr)
Exam 8.1.2007 13-16 S3
Please write clearly. Voit vastata myös **suomeksi**

1a) Consider a Gated Clock implementation where the clock to various logical modules can be individually turned off as shown in the figure below. (i.e., *Enable1,..., EnableN* can take on different values on a cycle by cycle basis). Which approach (*A* or *B*) results in lower *jitter* at the output of the input clock driver? (hint: consider gate capacitance) Explain. (2p)

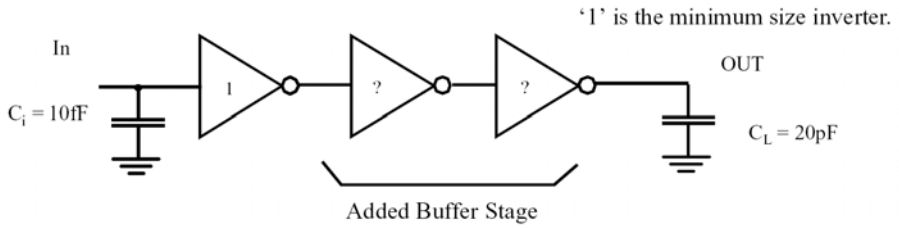


c) A balanced clock distribution scheme is shown below. For each source of variation, identify if it contributes to skew or jitter (explain). (4p)



c) For a technology scaling factor of s = 0.5, derive the relationship between gate delay and semi-global wire delay. Both the wire width and height scale by s and the capacitance of a semi-global wire can be thought of as a constant. (4p)

2 In order to drive a large capacitance (CL = 20 pF) from a minimum size gate with input capacitance Ci = 10 fF), you decide to introduce a two-staged buffer as shown in the figure below. Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume that the input capacitance of a gate is proportional to its size.

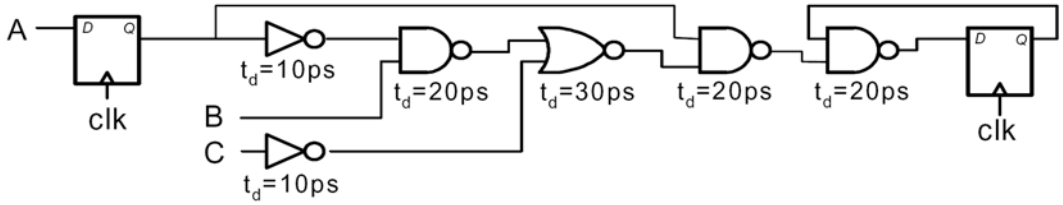


a) Determine the sizing of the two additional buffer stages that will minimize the propagation delay. (4p)

b) If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case? (4p)

c) Describe the advantages and disadvantages of the methods shown in a) and b). (2p)

3a) In the figure below A, B and C are primary inputs and you may assume they are available at t=0. The two flip-flops are driven by the same clock source. However, due to varying path lengths, there is possible skew between the clock inputs to the two flipflops. The parameters of the two flip-flops are: t_{dCQ} = 10ps, ts = 10ps, th = 20ps. Each gate has the delay listed in the figure. Find the maximum skew that the system can tolerate. With that maximum skew present, what is the maximum clock frequency at which this system can operate? (6p)



b) On chip clock distribution is easier than off chip clock distribution because the on-chip wires are of much higher quality (true or false, explain) (1p)?

c) Describe two methods (buffer placement, wiring) for efficient clock distribution. Explain the advantages and disadvantages of both methods. (3p)

4a) For a latch or flip-flop, explain the terms ts, th, ta, t_{dCQ}, and t_{cCQ}. (a diagram would be helpful here) (4p)

b) Draw a transistor-level schematic of a MUX-based latch and use this diagram to explain the physical causes of ts, th, and t_{dCQ}. (6p)