S-87.3190 Computer Architecture (5 cr) Exam 22.5.2013

Please write clearly. Voit myös vastata suomeksi.

Mark your project completion year / Merkitse harjoitustyön suorittamisvuosi

1. a) Explain the meaning of an Instruction Set Architecture (3p)
   b) Implement the following pseudo-instructions with MIPS instructions; (2p)

```
move $t1, $t2        # $t1 = $t2
clear $t1            # $t1 = 0
g = h + A[5]         # g: $s1, h: $s2, $s3:base address of A
```

   c)Explain the concept of program threads. (1p)
   c) Why are threads important in GPU systems. (1p)
   d) What is the meaning of N = 0b1101 if it is interpreted as a: (3p)
   - Sign/Magnitude number (write your answer in decimal);
   - Twos Complement number (write your answer in decimal);
   - Unsigned number (write your answer in decimal);
   - Float with SEEM format (1 Sign (S) bit, 2 Exponent (E) bits, 1 Significant (M) bit, bias = 1)

2. a) Explain how virtual memory functions. (3p)
   b) Suppose we have a write-back cache used for a processor with a bus and memory system with the following characteristics:
   1. A memory and bus system supporting block access of 4 to 16 32-bit words.
   2. A 64-bit synchronous bus clocked at 200 MHz, with each 64-bit transfer taking 1 clock cycle, and 1 clock cycle required to send an address to mem¬ory.
   3. Two clock cycles needed between each bus operation. (Assume the bus is idle before an access.)
   4. A memory access time for the first four words of 200 ns; each additional set of four words can be read in 20 ns.

   The following performance measurements have been made:
   - The cache miss rate is 0.05 misses per instruction for block sizes of 8 words.
   - The cache miss rate is 0.03 misses per instruction for block sizes of 16 words.
   - For either block size, 40% of the misses require a write-back operation, while the other 60% require only a read.

   Assuming that the processor is stalled for the duration of a miss (including the write-back time if a write-back is needed), find the number of cycles per instruction that are spent handling cache misses for each block size. (Hint: First compute the miss penalty.) (3p)

   c) Instead of using a special hardware multiplier, it is possible to multiply using shift and add instructions. This is particularly attractive when multiplying by small constants. Suppose we want to put nine times the value of $s0 into $s1, ignoring any overflow that may occur. Show a minimal sequence of MIPS instructions for doing this without using a multiply instruction. (4p)

TURN OVER =>

3. a) What does the concept forwarding mean? What for and how is it used in MIPS? What can be done when forwarding does not solve a problem? (3p)
b) In MIPS assembly, write an assembly language version of the following code segment:

```
int A[100], B[100];
for (i=1; i < 100; i++) {
A[i] = A[i-1] + B[i];
}
```

At the beginning of this code segment, the only values in registers are the base address of arrays A and B in registers $a0 and $a1. (7p)

4. Below is the single-cycle MIPS datapath presented during lecture. Your job is to modify the diagram for multicycle (pipelined) operation (7p)
b) Also explain how the control changes with multi-cycle operation (3p)