S-87.3190 Computer Architecture (5 cr) Exam 28.04.2014

Please write clearly. Voit myös vastata suomeksi.

Mark your project completion year / Merkitse harjoitustyön suorittamisvuosi

1. a) Prior to the early 1980s, machines were built with more and more complex instruction set. The MIPS is a RISC machine. Why has there been a move to RISC machines away from complex instruction machines? (2p)

   b) In MIPS assembly, write an assembly language version of the following code segment:

```
int A[100], B[100];
for (i=1; i < 100; i++) {
A[i] = A[i-1] + B[i];
}
```

   At the beginning of this code segment, the only values in registers are the base address of arrays A and B in registers $a0 and $a1. (5p)

   c) With the values in the table on the right (3p):

Instruction	Frequency	CPI
ALU	25%	1
Load	35%	3
Store	10%	5
Branch	30%	4

   1) What is the overall CPI?

   2) If Stores were free (CPI=0), how many times faster would the CPU be?

   3) If you could make one instruction type twice as fast, what should it be?

2. a) Explain the three MIPS instruction formats. (4p)

   b) The following MIPS instructions that are listed below are located at the memory location 0x70000008. Assume $t0 contains 0xDEADBEEF. What is the address of the next instruction that will be executed in each case? (6p)

   000010 11111 11100 00000 00000 000011 (= `j` instruction)

   000000 01000 00000 00000 00000 001000 (= `jr $t0`)

   000101 01000 00000 11111 11111 111110 (= `bne $t0, $zero, offset=-`2_{10})

   000000 00000 01000 01000 00000 100011 (= `subu $t0, $zero, $t0`)

3. Consider a variation on the canonical MIPS 5 stage pipeline, which doesn't have any forward paths, doesn't have branch delay slots, and resolves branches in the execute stage. For the following code sequence, answer all questions (2p each)

```
addu $t3, $t4, $t5
beq $t0, $t1, label
srlv $s0, $s1, $s2
addu $t4, $t4, $t4
```

   a) When $t0 != $t1, how many instruction fetches are wasted in the original processor?

   b) When $t0 == $t1, how many instruction fetches are wasted in the original processor?

   c) Assume the branches are resolved in the decode stage. When $t0 == $t1, how many instruction fetches are wasted?

   d) Assume the processor implements branch delay slots, and branches are resolved in the decode stage. Reorganize the code sequence to minimize number of wasted instruction fetches when $t0 == $t1.

TURN OVER =>

4. a) What type of hazards may happen in the operation of a pipeline? Explain the causes behind the different type of hazards and how the hazards are dealt with in MIPS. (4p)
b) Construct a single-cycle 32-bit datapath which can implement the two MIPS instructions ADDU, ORI (include bit-widths, explain control signals) (6p)