ELEC-E3520 Digital Microelectronics I, Exam 18.02.2016 Marko Kosunen/Antti Ontronen

Write your name and student number on every paper (also on possible appendices). All calculators allowed. No literature allowed.

OBS: Some points are given also from answers with incorrect numerical answers. The emphasis in symbolic calculations, i.e. showing that you understand what you are calculating.

1. a) You have a non-recursive arithmetic unit implemented with some register stages and static CMOS logic. Your computation speed is sufficient, but you should decrease your power consumption. What can you do? (3p)

b) What is the speed bottleneck of a digital adder? Give an example of adder structures used to overcome this problem. (3p)

2. a) Derive the logic functions for S and C_{out} of a one-bit full-adder with inputs A, B, and C_i. Use only AND, OR, and negation operators in your expressions. You can use whatever method you like (boolean algebra, Karnaugh maps, etc.). (2p)

b) Implement the functions required for the a)-part with a single static CMOS logic gate (at most followed by an inverter). Draw the transistor-level schematics of the gate. You can assume that both the direct and negated versions of each input are available. (2p)

c) In minimum sized inverter the PMOS/NMOS size ratio that produces equivalent rise and fall times is 2. Size all the devices in your logic gates so that the worst case ratio of rise and fall times is equal to minimum sized inverter. (Effect of internal node capacitances can be neglected). (2p)

3. Fig. 1 depicts a Master-slave register. a) Explain, in terms of voltage transitions at nodes D,

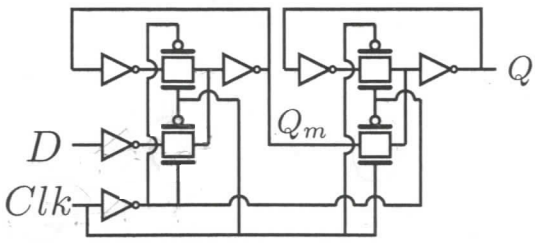

Figure 1

Clk, Q_m,a nd Q how the register works. (3p)

b) Explain in terms of voltage transitions at nodes D, Clk, Q_m, and Q what happens if *setup time* constraint of the register is violated. (3)