4. a) How the *effective fanout* f of an inverter is defined? (2p)

b) Derive the equation for the optimal effective fanout of a stage in inverter chain for buffering. (2p)

c) Use the good practical estimate for optimal effective fanout to obtain optimum number of stages for a inverter chain if the minimum sized inverter has input capacitance 1 and the load capacitance to drive is 256. Draw the inverter chain and load capacitance, and add the relative inverter sizes and the load capacitance value to the figure. (2p)

5. a) Describe the phenomenon that can cause errors when you transfer data over from one clock domain to another in case the clocks of the two different domains are asynchronous. (3p)

b) Describe methods to alleviate this problem. (3p)