ELEC-E8001 Embedded Real-Time Systems

EXAM 11.12.2015

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1. Are the following claims true (T) or false (F)? Every correct answer gives you +1 p, every incorrect –1 p, and an empty answer is worth 0 p. The minimum amount of total points is 0 p and maximum 6 p.

   a) If the CPU utilization factor is > 1, it does not necessarily mean that such a real-time system with multiple periodical tasks will miss one/some of its deadlines.
   b) From the CPU viewpoint, a divide-by-zero interrupt is a synchronous and sporadic event.
   c) Real-time punctuality is particularly important in periodically sampled systems with high sampling rates, for instance, in video signal processing.
   d) In cost-effective and robust real-time systems, a pragmatic rule of thumb could be: process everything as fast as possible and repeat tasks as often as possible.
   e) A system is a mapping of a set of inputs into a set of outputs.
   f) Real-time systems are always synonymous with "fast" systems.

2. In an embedded real-time system for some industrial control application, which combination of I/O technique to input/output assignments *makes the most sense* from a pure run-time performance (time efficiency) standpoint? (3 p) Explain the reasoning behind your answer (3 p). Only one alternative (a, b, c, d or e) is correct.

   a) Update a textual display via programmed I/O; Send a single command byte to a motor control unit via DMA; Receive 64 bytes of data from a data acquisition unit via DMA.
   b) Update a textual display via memory-mapped I/O; Send a single command byte to a motor control unit via programmed I/O; Receive 64 bytes of data from a data acquisition unit via DMA.
   c) Update a textual display via memory-mapped I/O; Send a single command byte to a motor control unit via DMA; Receive 64 bytes of data from a data acquisition unit via programmed I/O.
   d) Update a textual display via programmed I/O; Send a single command byte to a motor control unit via memory-mapped I/O; Receive 64 bytes of data from a data acquisition unit via memory-mapped I/O.
   e) Update a textual display with memory-mapped I/O; Send a single command byte to a motor control unit via DMA; Receive 64 bytes of data from a data acquisition unit via programmed I/O.

3. An embedded monitoring system is executing the application program `MAIN`. During the execution of the third instruction, the CPU receives an interrupt request from an A/D converter (interrupts are enabled). And the interrupt service routine `INTR` performs the necessary service for that interrupt. The CPU has a three-stage instruction pipeline (instruction FETCH, DECODE, EXECUTE), and each pipeline stage needs one clock cycle to complete. How many clock cycles after starting the application program it becomes fully executed? Assumption: initially the instruction pipeline is empty. (6 p)

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MAIN: Instruction 1          INTR: Instruction a
      Instruction 2                Instruction b
      Instruction 3                Instruction c
      Instruction 4                Instruction d
      Instruction 5                Instruction e
      Instruction 6
```

4. A preemptive priority system has three periodical tasks, described below. The task priorities are determined according to the rate-monotonic principle. Note: the "Execution Time" column does not contain the contribution of context switching.

Task Id.	Execution Period (ms)	Execution Time (ms)
τ_1	100	20
τ_2	20	5
τ_3	25	10

Now, considering that each context-switch takes 0.1 ms, draw the execution time line for this system. The time line begins at time instant "0" when all the tasks are ready to run and the highest-priority task is just starting its execution, and ends when all the tasks have been executed to completion at least once. (6 p)

5. A real-time system controls the production processes at an automated pasta sauce bottling facility. The real-time system is a preemptive priority one and consists of three real-time tasks and a background task. The task information is given in the table below:

Task	Function	Rate	Priority (1 is highest)
(I) `Alarm_processing`	Respond to exceptional and urgent events such as conveyor jam, dispenser malfunction, etc.	Aperiodic	1
(II) `Process_control`	Issue normal commands to automated equipment and collect line data for display	5 times per second	2
(III) `Screen_update`	Display control and process information to operator console monitor	40 times per second	3
(IV) `Background`	Data logging from process control information and system diagnostics	Always when there is CPU time available (background)	n/a

For which task pairs would you expect that a double buffering scheme would be needed to pass information (3 p)? Explain the reasoning behind your answer (3 p). Only one alternative (a, b or c) is correct.

a) I and IV.
b) I and II, II and IV.
c) II and III, II and IV, III and IV.