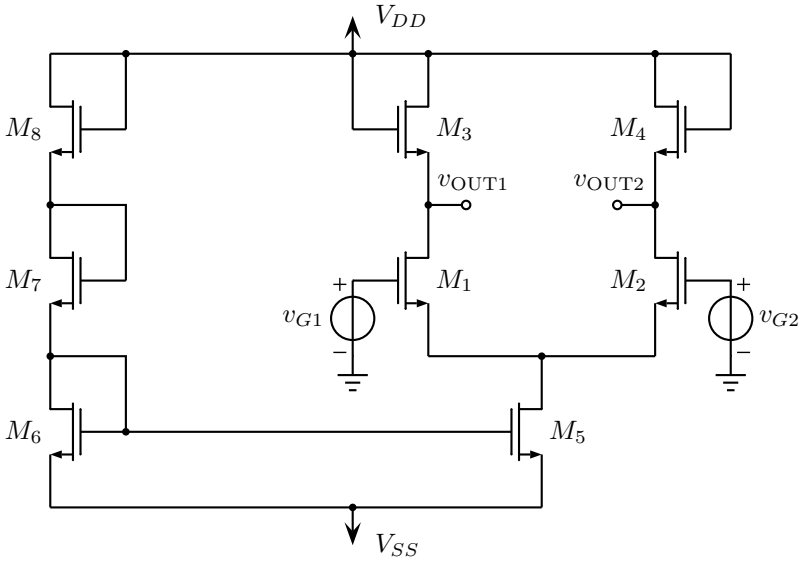
This exam includes five problems. Note that the last one is at the other side of the paper. Each problem gives 10 points at maximum.

1.

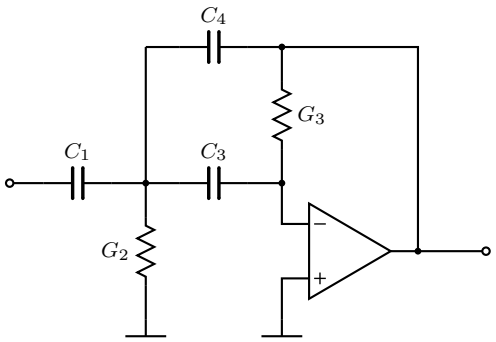
Answer shortly with few words to the following questions.
a) How and why do you use a small-signal model to analyze a nonlinear circuit? (4p)
b) If you want to achieve good impedance matching, where your curve should be on the Smith chart? (3p)
c) To convert analog signals into a digital form, we do sampling, which can affect aliasing if not done properly. Why and what does it mean? (3p)

2.

a) What parts does this circuit have?
b) Draw the small signal model for this circuit. Assume that all transistors are in saturation.



3.



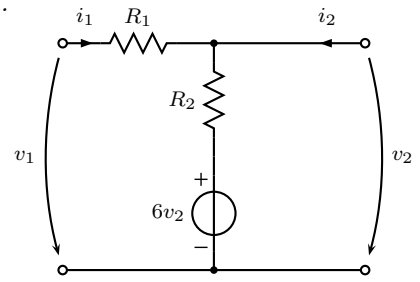
The voltage transfer function for the circuit in the figure

$$H(s) = -\frac{s^2 C_1 C_3}{s^2 C_3 C_4 + sG_3\left(C_1 + C_3 + C_4\right) + G_2 G_3}.$$

a) What is the type of the frequency response for the circuit?
b) At what frequency is the voltage gain maximum?
c) What is the maximum value of the gain?
d) What is the Q value of the circuit?

$$H(s) = \frac{p(s)}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2}$$

4.



Determine the hybrid parameters of the circuit.

$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0} \qquad h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0}$$

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0} \qquad h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0}$$

$$R_1 = 2\ \Omega \quad R_2 = 3\ \Omega.$$

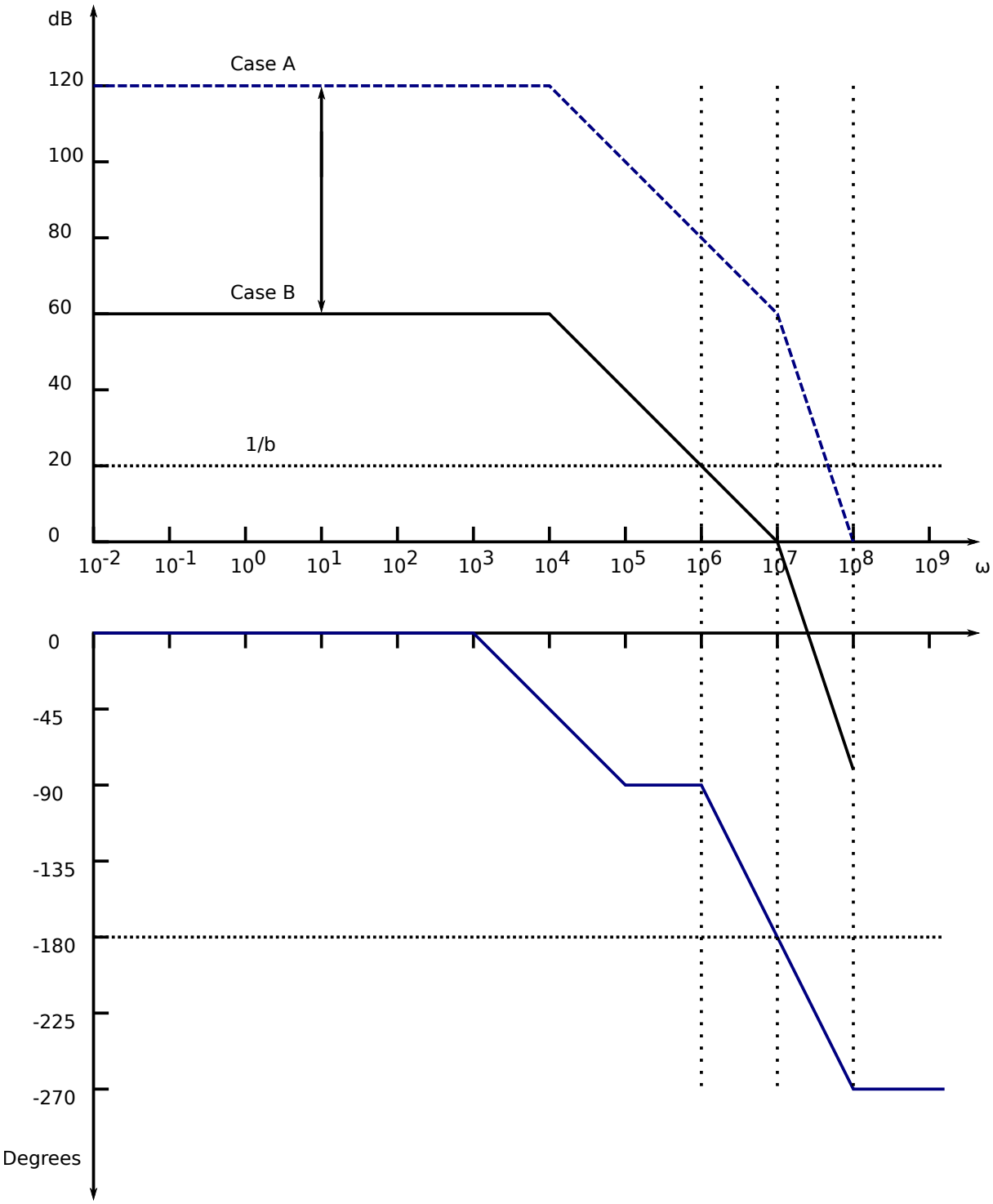
5.

The figure shows the Bode plots for two negative-feedback amplifiers. Answer shortly to following questions.

a) What is the DC gain, phase margin, gain margin, and unity gain frequency in case A (dashed line)? (4 p)

b) We want to use amplifier in case A to construct a stable amplifier with a closed-loop gain of 20 dB. Therefore, we lower the open-loop gain as shown in case B. What is the DC gain, phase margin, gain margin, and unity gain frequency in this modified case B (solid line)? (4 p)

c) In order to make the system stable, instead of using the method applied for case B, we could modify the poles by moving or adding them to lower frequencies. What is the drawback of this method? (2 p)



0.1

Answer shortly with few words to the following questions.
a) How and why do you use a small-signal model to analyze a nonlinear circuit? (4p)
b) If you want to achieve good impedance matching, where your curve should be on the Smith chart? (3p)
c) To convert analog signals into a digital form, we do sampling, which can affect aliasing if not done properly. Why and what does it mean? (3p)

---

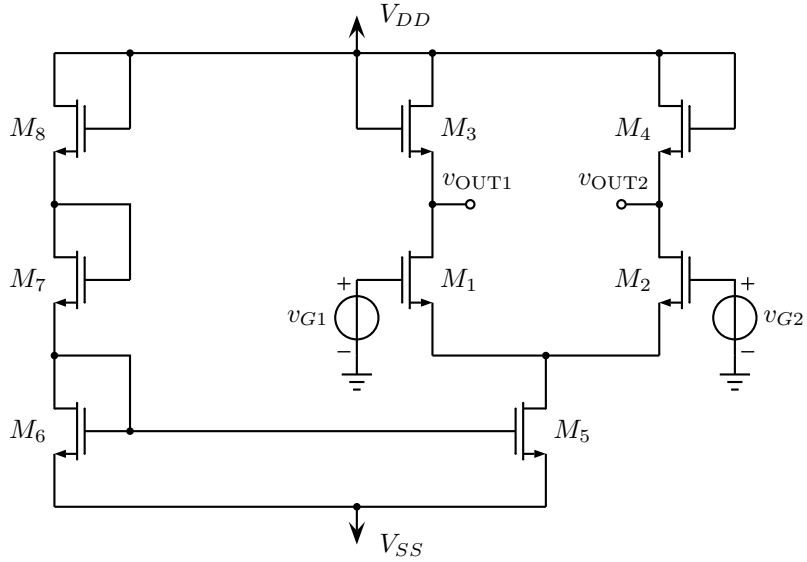
a) Nonlinear circuits are difficult to analyze. However, if the changes in a signal level are small so that we are near the DC operating point and the state of the nonlinear device doesn't change, the nonlinear circuit can be linearized, i.e. a nonlinear model is replaced with a linear one. Linear circuits are much easier to analyze.

b) The center (origin) of the Smith chart corresponds to the reflection coefficient being zero.

c) An analog signal is converted to digital by taking discrete samples. Aliasing occurs when a signal is digitized at an insufficient sampling rate. The delay between the samples is too long compared to the highest frequency. Then different signals become indistinguishable when sampled and a part of the information is lost.

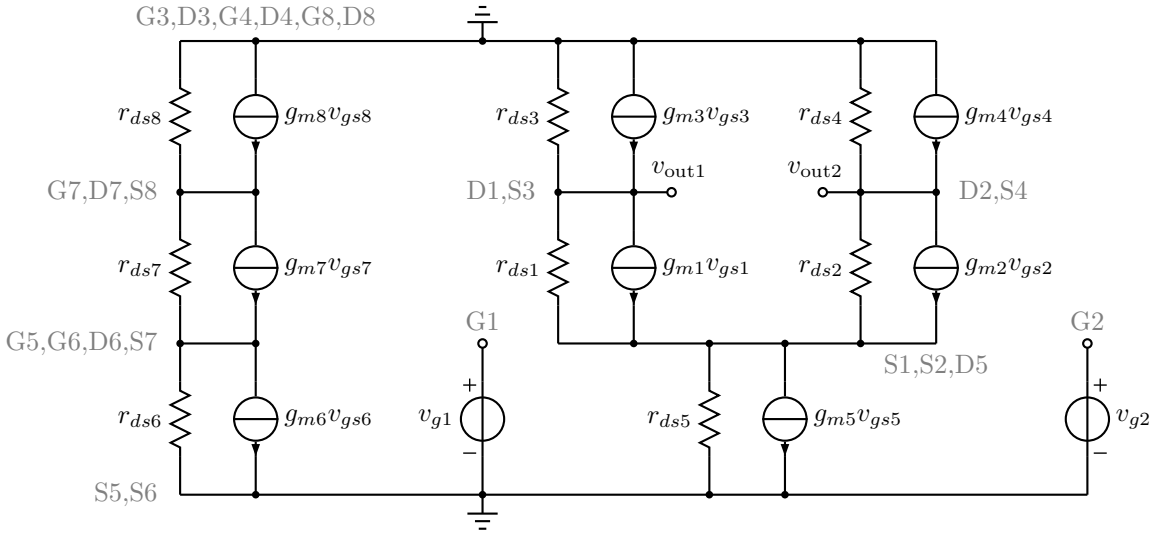
0.2

a) What parts does this circuit have?
b) Draw the small signal model for this circuit. Assume that all transistors are in saturation.

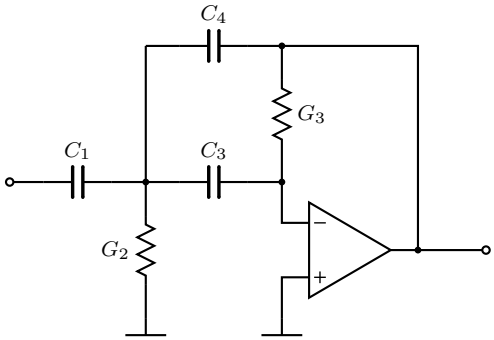


---

a) The parts are:
M_1 and M_2: differential pair (NMOS).
M_3 and M_4: active load for the differential pair (pull-up loads).
M_5 and M_6: current mirror (NMOS).
M_7 and M_8: current mirror reference.
b) In the figure below every transistor has been drawn, even though some of them (which ones?) will not have an effect on the small signal behavior. We will look at it better next week, for now it is enough to get this figure drawn. (Also, you need to remember to calculate the parameters g_m's and r_{ds}'s for all the needed ones.)



0.3



The voltage transfer function for the circuit in the figure

$$H(s) = -\frac{s^2 C_1 C_3}{s^2 C_3 C_4 + sG_3\left(C_1 + C_3 + C_4\right) + G_2 G_3}.$$

a) What is the type of the frequency response for the circuit?
b) At what frequency is the voltage gain maximum?
c) What is the maximum value of the gain?
d) What is the Q value of the circuit?

$$H(s) = \frac{p(s)}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2}$$

This question was actually ambiguous, which was not originally the purpose (items b and c).

$$H(s) = -\frac{s^2 C_1 C_3}{s^2 C_3 C_4 + sG_3\left(C_1 + C_3 + C_4\right) + G_2 G_3}.$$

a) This is a high-pass filter (both zeros are at the origin).

d)

$$\Delta\omega = \frac{\omega_0}{Q} = \frac{G_3(C_1 + C_2 + C_3)}{C_3 C_4}$$

$$Q = \frac{C_3 C_4}{G_3(C_1 + C_2 + C_3)} \cdot \omega_0 = \frac{\sqrt{C_3 C_4 G_2}}{\sqrt{G_3}(C_1 + C_2 + C_3)}$$

For items b and c, there are two ways to answer:

b) The voltage gain maximum is when the frequency approaches infinite.

c)

$$|H(s \to \infty)| = \frac{C_1 C_3}{C_3 C_4} = \frac{C_1}{C_4}$$

Another correct answer:
b) The voltage gain maximum is at corner frequency ω_0 (if $Q > 1$).

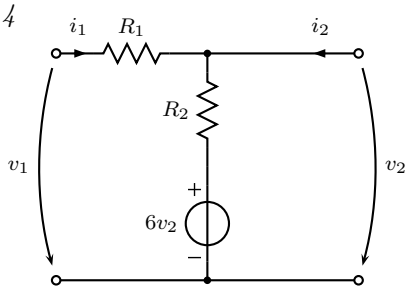
$$\omega_0 = \sqrt{\frac{G_2 G_3}{C_3 C_4}}$$

c)

$$|H(\omega_0)| = \frac{C_1 C_3 \omega_0}{G_3(C_1 + C_2 + C_3)} = \sqrt{\frac{G_2 G_3}{C_3 C_4}} \cdot \frac{C_1 C_3}{G_3(C_1 + C_2 + C_3)} = \sqrt{\frac{G_2 C_3}{G_3 C_4}} \cdot \frac{C_1}{C_1 + C_2 + C_3}$$

So, both answers to b and c are correct, but the answer cannot be combination of both.

0.4



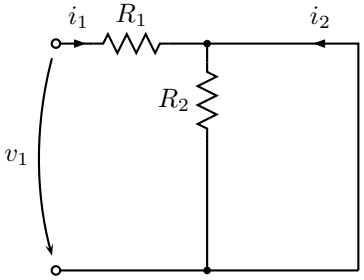
Determine the hybrid parameters of the circuit.

$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0} \qquad h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0}$$

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0} \qquad h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0}$$

$$R_1 = 2\ \Omega \quad R_2 = 3\ \Omega.$$

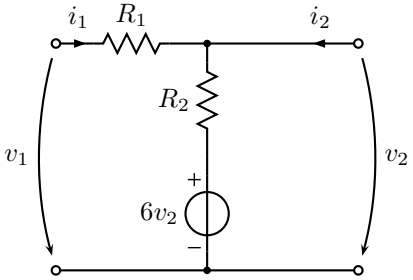
Assume $V_2 = 0$:



$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0} R_1 = 2$$

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0} = -1$$

Assume $I_1 = 0$:



$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0} = 1$$

From figure

$$v_2 = R_2 i_2 + 6v_2 \quad \Rightarrow \quad 5v_2 = -R_2 i_2$$

$$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0} = \frac{-5}{R_2} = -\frac{5}{3}$$

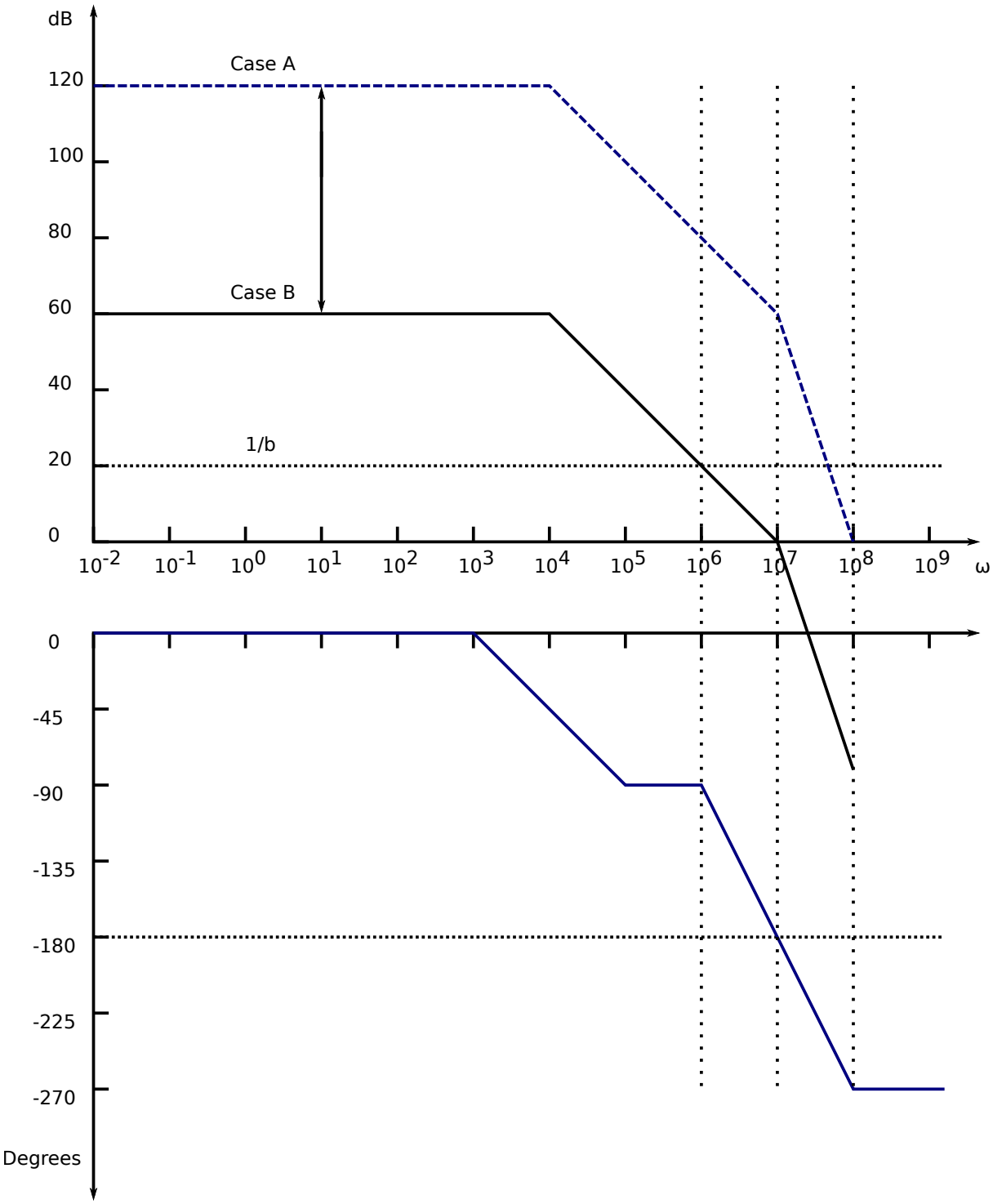
0.5

The figure shows the Bode plots for two negative-feedback amplifiers. Answer shortly to following questions.

a) What is the DC gain, phase margin, gain margin, and unity gain frequency in case A (dashed line)? (4 p)

b) We want to use amplifier in case A to construct a stable amplifier with a closed-loop gain of 20 dB. Therefore, we lower the open-loop gain as shown in case B. What is the DC gain, phase margin, gain margin, and unity gain frequency in this modified case B (solid line)? (4 p)

c) In order to make the system stable, instead of using the method applied for case B, we could modify the poles by moving or adding them to lower frequencies. What is the drawback of this method? (2 p)



---

a) In case A, the DC gain is 120 dB, the phase margin is -90 degree indicating unstable case. The gain margin is

-60 dB (in practice, zero) and unity gain frequency is 100 Mrad/s. (This case is the most right vertical dashed line.)

b) In case B, the DC gain is (60-20)=40 dB, the phase margin is 90 degree. The gain margin is 20 dB and unity gain frequency is 1 Mrad/s. (This case is the most left vertical dashed line.)

c) If poles are at lower frequencies, the gain starts to drop at lower frequencies and the obtainable bandwidth decreases.