ELEC-E3520 Digital Microelectronics I, Exam 21.02.2019 Vishnu Unnikrishnan

Write your name and student number on every paper (also on possible appendices). Return also this exam sheet. All calculators allowed. No literature allowed.

OBS: Some points are given also from answers with incorrect numerical answers. The emphasis in symbolic calculations, i.e. showing that you understand what you are calculating.

1. a) Derive the logic functions for sum s and carry output c_{out} of a full-adder with inputs a, b, and c_i. You may use whatever method you like (boolean algebra, Karnaugh maps, etc.) in the derivation of the logic functions. (3p)

b) To support transistor-level implementation, rewrite the equations with only AND, OR, and negation operators in case the expressions from a) used XOR, XNOR etc. (1p)

c) Implement s and c_{out} at transistor-level with two static CMOS logic gates respectively. Draw the transistor-level schematics of the gates. You can assume that both the direct and inverted versions of input are available. (4p)

d) For a minimum sized inverter, the PMOS/NMOS size ratio that produces equivalent t_{PLH} and t_{PHL} is 2. Size the devices in your logic gates so that the *worst case* rise and fall times are equal to a minimum sized inverter. Effect of internal node capacitances can be neglected. (2p)

2. Consider the pipeline shown in Figure 1. The flip-flops have the following properties: $t_{clk\text{-}q}$ = 150 ps, t_{setup} = 50 ps, and t_{hold} = 100 ps. The circuit is clocked at 1 GHz. You can assume that the clock has no jitter, but t_{skew} can be either positive or negative.

a) Calculate the maximum and minimum propagation delay allowed for CL_1 that will result in a functional circuit, when t_{skew} = 80 ps. (4p)

b) Calculate the maximum and minimum propagation delay allowed for CL_2 that will result in a functional circuit, when t_{skew} = –100 ps. (4p)

c) The dynamic power consumption of the circuit is 0.4 mW from a 1.0V supply. You observe that you can safely decrease the supply voltage to 0.8V, without compromising circuit operation at 1 GHz. What is the dynamic power consumption with the decreased supply? (2p)

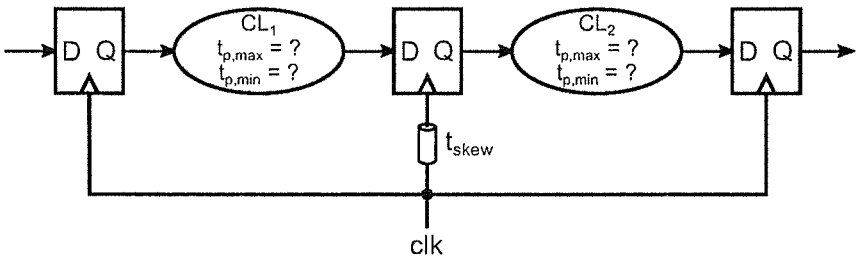

Figure 1: Pipeline with skewed clock distribution.

3. Consider the task of adding two 16-bit integers. Full adders and multiplexers are available as building blocks. For each of the following adder architectures, (i) sketch the block diagram, (ii) indicate the critical path in the calculation of the sum, and (iii) derive the expression for the critical path delay for sum as a function of t_{FA}, $t_{FA,carry}$, and t_{MUX}. t_{FA} is the delay of the sum as well as the carry output of the full adder from a and b inputs. $t_{FA,carry}$ is the delay of the sum and the carry output of the full adder from the carry input (assume $t_{FA,carry} < t_{FA}$). t_{MUX} is the delay of the multiplexers. You may assume that the group propagate signals are available as output from the 4-bit RCA blocks.

a) Ripple-carry adder (RCA). (2p)

b) Carry-bypass adder built with 4-bit RCA blocks. (4p)

c) Carry-select adder built with 4-bit RCA blocks. (4p)

4. Fig. 2 depicts a recursive digital filter. Transfer function of the filter is

$$y(n) = ax(n) + by(n-1).$$

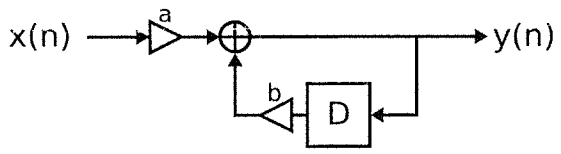

Figure 2

a) What is the critical path delay of the circuit if a coefficient multiplication takes t_c and a two input addition takes t_{add}? Assume that the sequential circuits are ideal ($t_{clk-q} = t_{setup} = t_{hold} = 0$) (1p)

b) Perform loop unfolding by a factor of 2. Draw the block diagram of the loop-unfolded filter. (4p)

c) Assuming that any constant multiplication takes t_c (use this opportunity to combine cascaded coefficient multipliers, if any, to minimize delay), what is the critical path delay for the loop-unfolded circuit? (2p)

d) Quantify the speed benefit of the new circuit, if any. (3p)