Microfabrication (CHEM-E5115) exam August 11th, 2017

Answer 5 out of 6 questions. All questions 6 point max. If you answer all, 6, the best one will be dropped out.

Make sure your answers are coherent and consistent: a collection of facts is not an answer.

You have to argue for your choices: there is usually more than one way of doing things, and therefore you have to give reasons for doing things your way.

Draw figures and graphs when appropriate.

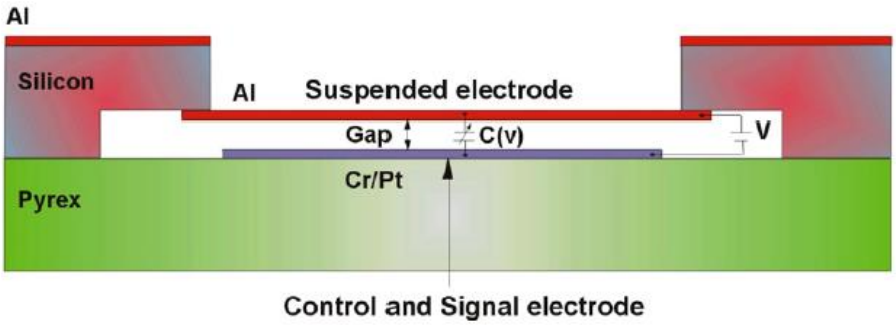
Note that some features in the drawings are because of drawing software only and do not represent actual microfabrication profiles.

Answer using pencil, or if you use pen, make sure to sketch your answer properly on a non-official paper before writing it down to official exam paper to avoid overwriting.

Start answer to each question from top of a new page. The first sheet contains pages 1-4, page 5 is the front page of the second sheet.

1. Give a short but concise description which deposition and patterning processes are used to make the metallizations listed below. For each case you must only discuss one method, the one that you think is best suited for this application. (1 p. each).
   HINT: you should only spend 6 minutes for each!
   a) copper metallization for 32 nm CMOS
   b) aluminum metallization for 0.8 µm CMOS
   c) 50 µm wide, 5 µm thick copper lines for a solar cell current collectors
   d) 3 µm wide, 500 nm thick doped polysilicon lines for a precision resistor
   e) 10 µm wide, 50 nm thick molybdenum lines for a heater resistor
   f) 50 nm wide, 50 nm thick silver lines for study of Ohm's law validity

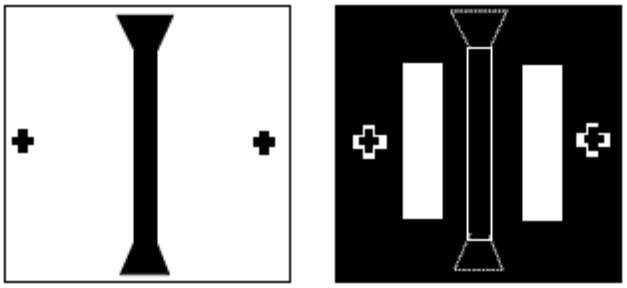
2. Write a short essay on wafer bonding, 3 points.
   Explain step-by-step the main fabrication steps of the capacitor shown below, concentrating on bonding. Discuss which process steps affect gap control. Give your estimates of device dimensions. 3 points.



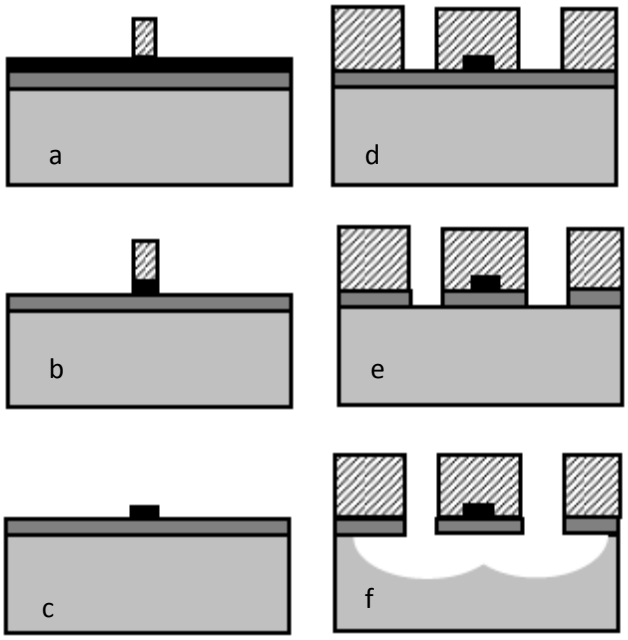
3. Analyze the fabrication process of the bolometer shown below step-by-step.3 points.

   Explain lithographic issues related to device: linewidths, alignment, etc. Assuming the figures are drawn to scale, give your estimates for lithographic and etched dimensions. 3 points.

   Hints: In the cross sectional views the black material is a conductor, the dark grey an insulator, light gray is silicon wafer, hatched material is photoresist.



Top views of photomasks



Sideviews of wafer processing

4. Identify the six different deposition processes shown below. Shortly discuss the prominent features of these deposition processes. 1 point each.

   a) SiH_4 (g) ➔ Si (s) + 2 H_2 (g)

   b) WF_6 (g) + 3H_2 (g) ➔ W (s) + 6 HF (g)

   c) CH_4 (g) ➔ C (s) + 2H_2 (g)

   d) $HfCl_4$ (ad) + 2 H_2O (ad) ➔ HfO_2 (s) + 4 HCl (g)

   e) $Au(CN)_2^-$ <=> AuCN + CN^-

      AuCN + e^- ➔ Au (s) + CN^-

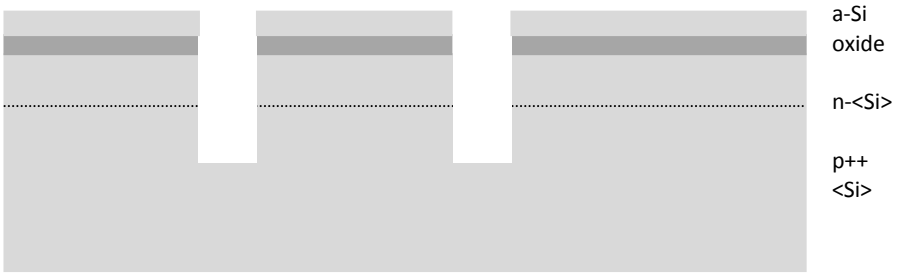
   f) F_3C-$(CF_2)_n$-Si-OH + HO-Si (surf) ➔ F_3C-$(CF_2)_n$-Si-O-Si (surf) + H_2O

5. Explain step-by-step how the structure shown below was made. 3 points. Answer to this part on regular answer sheet.

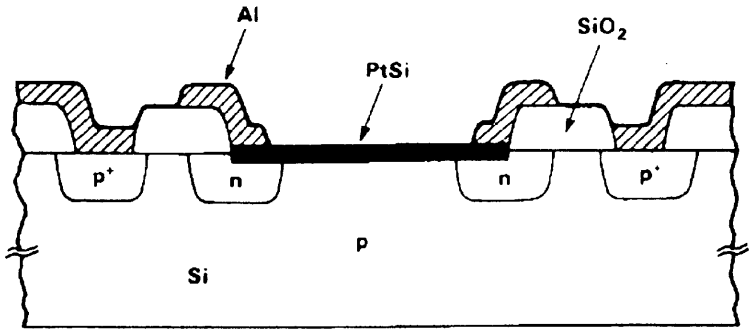
   Then consider six different continuation possibilities (separate cases; not a sequence); 0.5 point each. Both draw **TO SCALE** and explain key issues in words. Use separate answer sheet provided.

   a) annealing in N_2 at 1000°C for 1 hour
   b) oxidation at 1000°C for 1 hour
   c) in $POCl_3$ containing atmosphere at 1000°C for 1 hour
   d) KOH etching for 1 min at 80°C
   e) HF etching for 3 min
   f) LPCVD nitride deposition 500 nm

   Note: the figure is drawn to scale: n-<Si> epilayer is 1 µm thick and the trenches are 1 µm wide. Wafer thickness, however, is not to scale, but please ignore processes on backside.

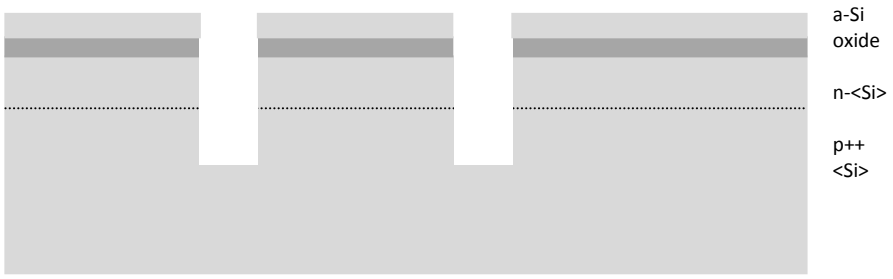


6. Explain step-by-step the fabrication of the photodiode shown below. 6 points.
   Hints: doping is done by ion implantation. Silicide is formed by solid state reaction between metal and silicon.



Return this answer sheet: Name:_____

a) annealing in N_2 at 1000^{o}C for 1 hour



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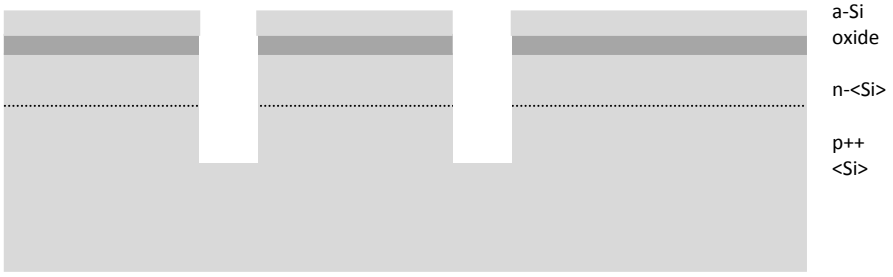
b) oxidation at 1000^{o}C for 1 hour



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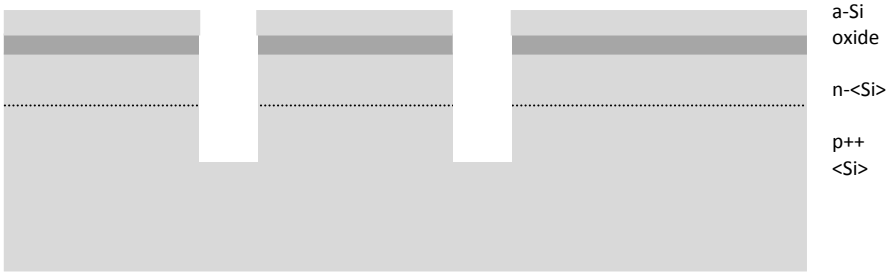
c) in $POCl_3$ containing atmosphere for one hour at 1000^{o}C



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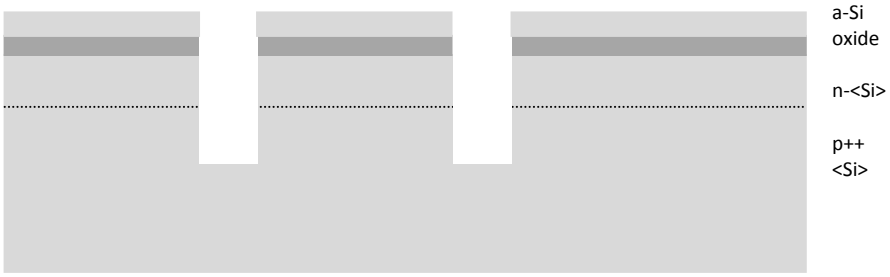
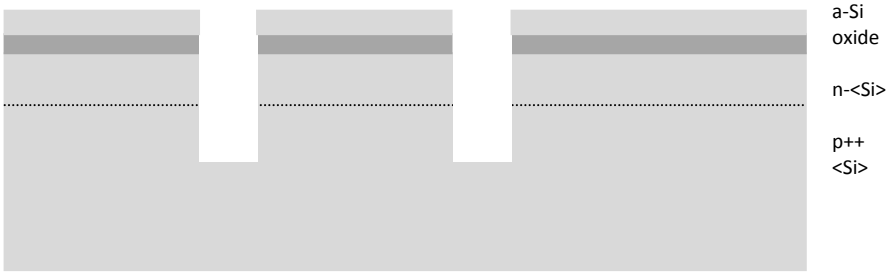
d) KOH etching for 1 min at 80^{o}C



e) HF etching for 3 min



f) LPCVD nitride deposition 500 nm