ELEC-E8001 Embedded Real-Time Systems

FINAL EXAM December 08, 2020

The exam has totally 70 points. The exam is an online exam, you may use references, but you should carry out the exam independently. Discussion with others is forbidden. All notations should be based on the course textbook unless specified otherwise. The written results (either clear handwriting or typed text) should be submitted online through MyCourses.

1. Are the following claims true (T) or false (F)? Every correct answer gives you +2 p, every incorrect –2 p, and an empty answer is worth 0 p. The minimum amount of total points is 0 p and maximum 10 p.
   a) In cost-effective and robust real-time systems, a pragmatic rule of thumb could be: process everything as slowly as possible and repeat tasks as often as possible.
   b) In real-time control systems, deadlines are based on the underlying physical phenomena of the system under control.
   c) A task is an abstraction of a running program and is the logical unit of work schedulable by the real-time operating system.
   d) Speculative execution works well with instruction pipelines if the locality of reference remains low.
   e) DRAM cannot keep the data in its cells when the power is uninterrupted without refreshing the data in the cell periodically.

2. Show with an example of a sequence of assembly-language instructions how the five-stage pipeline discussed in Chapter 2 (Figure 2.10, page 45) could benefit from the Harvard architecture? (5p)

3. You have an ancient 8-bit CPU with the instruction set given below. The following assembly-language program is written using that instruction set. b) What is the content of register R1 after the program is executed? Please explain your answer briefly. (10 p)
   Can you find a bug in the code? Please indicate. (5p) Can you simplify the code? If yes, please suggest the simplified code. (5 p)

Assembly Instruction	First byte		Second byte		Operation
MOV Rn, direct	0000	Rn	direct		Rn = M(direct)
MOV direct, Rn	0001	Rn	direct		M(direct) = Rn
MOV @Rn, Rm	0010	Rn	Rm		M(Rn) = Rm
MOV Rn, #immediate	0011	Rn	immediate		Rn = immediate
MOV Rn, Rm	0100	Rn	Rm		Rn = Rm
ADD Rn, Rm	0101	Rn	Rm		Rn = Rn + Rm
SUB Rn, Rm	0110	Rn	Rm		Rn = Rn – Rm
JZ Rn, relative	0111	Rn	relative		PCR = PCR + relative (only if Rn is 0)

Instruction set

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0       MOV R0, #0;
1       MOV R1, R0;
2       MOV R2, #7;
3       MOV R3, #95;
4       MOV R4, R0;
5       MOV R5, R0;
Loop:   MOV R0, R4;
7       ADD R0, R2;
8       MOV R4, R0;
9       ADD R1, R2;
10      SUB R0, R3;
11      JZ R0, Next;
12      JZ R5, Loop;
Next:   MOV R5, #1024
14      MOV @R5, R1
```

Program

Note: #n represents decimal number n

4. A given hardware design with an instruction cache has a program-memory access cost of 3 clock cycles on a hit and 15 cycles on a miss. A competing design without the cache has a program-memory access cost of 10 cycles. Calculate the minimum hit ratio (%) of the cache to make the cache implementation worthwhile. (5 p)

5. Construct a cyclic code structure with four tasks, communicate, destination, drive&door, and supervision. Task communicate runs three times as frequently as destination and drive&door, and task communicate runs four times as frequently as supervision. (5 p)

6. Considering a preemptive-priority RTOS and an embedded system with separate measurement channels for pressure and temperature, as well as a single A/D converter to be used by Tasks τ_1 and τ_2 for periodically

measuring those two quantities. Before starting an A/D conversion, the desired measurement channel must be selected. How would you share the serially reusable resource safely with τ_1 (high priority) and τ_2 (low priority)? Give your answer in a few lines of program code for both of the tasks using, for instance, C-like syntax. Define all the operating system services and other functions that you may use. (10 p)

7. A preemptive priority system has three periodically executed tasks, τ_1, τ_2 and τ_3, with required execution periods of p_1 = 15 ms, p_2 = 5 ms and p_3 = 20 ms, respectively. The corresponding worst-case execution times of those tasks are e_1 = 5 ms, e_2 = 1 ms and e_3 = 8 ms.
   Please draw a scheduling diagram to illustrate how the three tasks are scheduled according to the Rate-Monotonic (RM) principle, assuming all tasks are ready at time 0 and the worst-case execution times. Do you see any problem in the schedule, and why? (15 p)