ELEC-E3520 Digital Microelectronics I, Exam 25.02.2021 Marko Kosunen

Write your name and student number on every paper (also on possible appendices). All calculators allowed. No literature allowed.

OBS: Some points are given also from answers with incorrect numerical answers. The emphasis in symbolic calculations, i.e. showing that you understand what you are calculating.

1. In your design you have two register stages and non-recursive multistage logic in between. The setup time of the register is $t_s = 0.1$ ns and propagation delay $t_{CQ} = 0.5$ ns. The propagation delay through the logic $T_{pL} = 10$ ns is evenly distributed over the stages. Clock tree is ideal.

a) What is the maximum clock frequency you can use. (1p)

b) Your clock frequency target is $400MHz$. What you can do to enable this higher clockrate? Delays of single stage (logic or asynchronous stage) is considered negligible. (hint: two solutions)? (4p)

c) Answer shortly, how the situation is different if the logic contains feedback loops. Name the method that you can consider as a solution in this case. (1p)

2. a) Derive the logic functions for S and C_{out} of a one-bit full-adder with inputs A, B, and C_i. Use only AND, OR, and negation operators in your expressions. You can use whatever method you like (boolean algebra, Karnaugh maps, etc.). (2p)

b) Implement the functions required for the a)-part with a single static CMOS logic gate (at most followed by an inverter). Draw the transistor-level schematics of the gate. You can assume that both the direct and negated versions of each input are available. (2p)

c) In minimum sized inverter the PMOS/NMOS size ratio that produces equivalent rise and fall times is 2. Size all the devices in your logic gates so that the worst case ratio of rise and fall times is equal to minimum sized inverter. (Effect of internal node capacitances can be neglected). (2p)

3. Fig. 1 depicts a Master-slave register. a) Explain, in terms of voltage transitions at

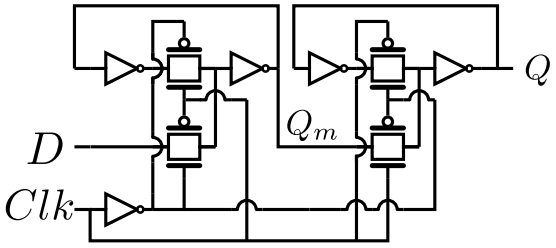

Figure 1

nodes D, Clk, Q_m,a nd Q how the register works. (3p)

b) Explain in terms of voltage transitions at nodes D, Clk, Q_m, and Q what happens if *setup time* constraint of the register is violated. (3)

4. a) How the *effective fanout* f of an inverter is defined? (2p)

b) Derive the equation for the optimal effective fanout of a stage in inverter chain for buffering. (2p)

c) Use the good practical estimate for optimal effective fanout to obtain optimum number of stages for a inverter chain if the minimum sized inverter has input capacitance 1 and the load capacitance to drive is 256. Draw the inverter chain and load capacitance, and add the relative inverter sizes and the load capacitance value to the figure. (2p)

5. a) Describe how the effect of timing violations can be alleviated in asynchronous clock domain crossing. (2p)

b) Describe the operation principle of how First-in-first-out (FIFO) buffer can be used in clock domain crossing.(4p)