ELEC-E3520 Digital Microelectronics I, Exam 23.02.2022 Marko Kosunen

Write your name and student number on every paper (also on possible appendices). **Use pencil**. All calculators allowed. No literature allowed.

OBS: Some points are given also from answers with incorrect numerical answers. The emphasis in symbolic calculations, i.e. showing that you understand what you are calculating.

1. a) You have a non-recursive arithmetic unit implemented with some register stages and static CMOS logic. Your computation speed is sufficient, but you should decrease your power consumption. What you can do? (3p)

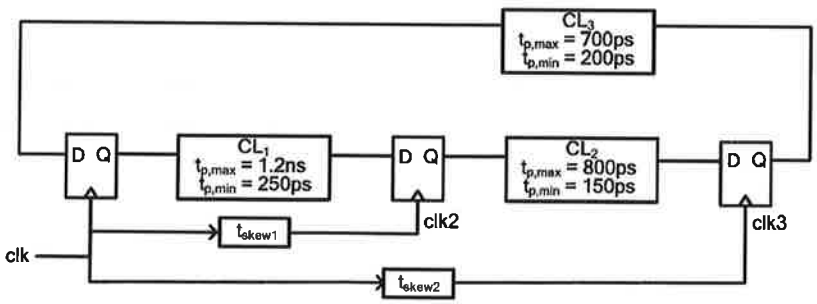
b) What is the speed bottleneck of a digital adder? Give an example of a adder structures used to overcome this problem. (3p)

2. Examine the pipeline shown below. The minimum and maximum delays through the logic are annotated on the figure, and the flip-flops have the following properties: t_{clk-q} = 150 ps, t_{setup} = 50 ps, and t_{hold} = 100 ps. You can assume that the clock has no jitter, but t_{skew1} and t_{skew2} can be either positive or negative.

a) What is the minimum clock cycle time if t_{skew1} = -100 ps and t_{skew2} = 50 ps? (1p)

b) Assuming t_{skew2} is fixed at 50 ps, how negative can t_{skew1} be before this pipeline fails a hold-time constraint? (2p)

c) If you could intentionally set the values of t_{skew1} and t_{skew2}, what values would you choose in order to minimize the cycle time of this pipeline? What would be the cycle time in this case? (3p)



3. How the *effective fanout* f of an inverter is defined? (2p)

b) What is a value of f that is considered a good trade-off in practical buffer designs? This value is also obtained by rounding up the optimal f value obtained for output capacitance factor $\gamma = 1$. (2p)

c) Use your answer for b-part to obtain optimum number of stages for a inverter chain if the minimum sized inverter has input capacitance 1 and the load capacitance to drive is 256. Draw the inverter chain and load capacitance, and add the relative inverter sizes and the load capacitance value to the figure. (2p)

4. Fig. 1 depicts a recursive digital filter. Transfer function of the filter is

$$y(n) = ax(n) + by(n-1).$$

a) In order to make re-timing possible, perform loop unfolding by factor of 2. Draw the block diagram of the loop-unfolded filter. (3p)

b) Examine the block diagram and consider, what possibilities loop unfolding provides for power consumption-computation speed trade-off. (3p)

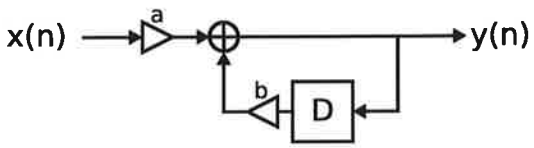


Figure 1

5. a) Draw the truth tables and schematics for inverter and 2-input NAND, NOR and XOR gates implemented with static CMOS.

b) Assume the channel length L is fixed. If the optimal size ratio of PMOS and NMOS transistors in the inverter is 2, how the sizes of the transistors in 2-input NAND, NOR and XOR should be chosen in order to maintain the propagation delay for the fixed load capacitance C_L.

(Total 6p)