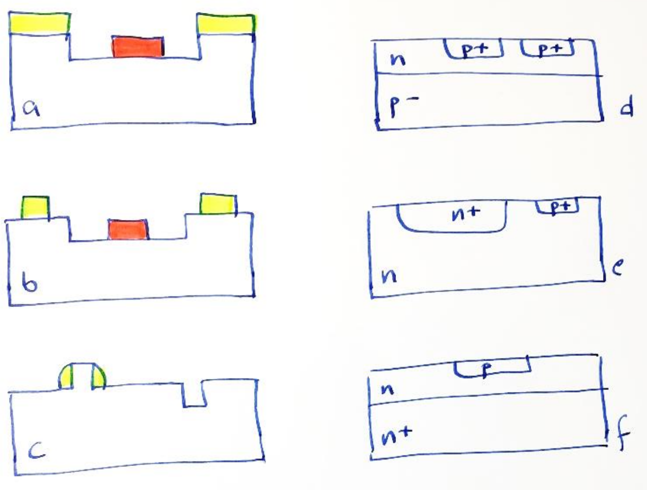
Microfabrication (CHEM-E5115) exam June 2, 2023, 9.00-12.00

- *There are 6 other questions, answer 5 of them. If you answer all 6, the best one will be dropped out.*
- *All questions are 6 points.*
- *Normal scientific quotation practices are in effect. SUBMITTING TEXT WRITTEN BY SOMEBODY ELSE AS YOURS IS A SERIOUS VIOLATION OF AALTO CODE OF CONDUCT. This applies to AI-assisted text as well.*
- *Make sure your answers are coherent and consistent: a collection of facts is not an answer.*
- *There is usually more than one way of doing things, so you have to argue for your choices.*
- *Draw figures and graphs when appropriate. Take a photo of hand drawn figure and embed it in text-document.*
- *Note that some features in the drawings are because of drawing software only and do not represent actual microfabrication profiles.*
- *Return each answer as a separate pdf-file into return boxes 1-6. Put your name on top of the page in every pdf.*

1.Step-by-step processes:

Use only the following process steps to explain step-by-step fabrication of structures shown in a-f. 1 p. each.

THERMAL OXIDATION
LITHOGRAPHY
ETCHING MATERIAL X (+STRIP)
DIFFUSION N/P TYPE
EPITAXY N/P TYPE
DEPOSITION OF FILM X



2a. Anodic bonding. Please read the essay “Anodic bonding in MEMS”. Correct it where needed and add quantitative details to it. 3 points.

Anodic bonding is a widely used technique in the field of Microelectromechanical Systems (MEMS) for hermetic sealing and bonding of glass or silicon-based materials. This bonding method involves the fusion of two substrates under the influence of an electric field at an elevated temperature.

In the anodic bonding process, one substrate typically contains a layer of glass, while the other substrate is usually made of silicon. The glass substrate serves as an insulating material, while the silicon substrate provides mechanical strength and electrical functionality. Prior to bonding, the surfaces of the substrates are carefully prepared to ensure cleanliness and compatibility.

During bonding, the glass and silicon substrates are pressed together under high voltage and elevated temperature conditions. An electrical potential is applied across the substrates, creating an electric field that induces ion migration and electrostatic attraction at the interface. As a result, the atoms from the glass substrate migrate towards the silicon substrate, forming strong covalent bonds.

Anodic bonding offers several advantages for MEMS devices. It provides excellent hermetic sealing, preventing the ingress of moisture and contaminants. The bond strength is high, ensuring robust device integrity. Moreover, anodic bonding allows for the integration of dissimilar materials, enabling the combination of different functionalities in a single device.

However, anodic bonding also presents some challenges. It requires precise control of process parameters, including temperature, voltage, and time, to achieve successful bonding and avoid structural deformations.

2b. Fusion bonding. Please read the essay “Fusion bonding in silicon technology”. Correct it where needed and add numerical details to it. 3 points.

Fusion bonding is a key process utilized in silicon technology to create strong and permanent bonds between two silicon wafers or substrates. It involves joining two separate silicon surfaces at the atomic level, resulting in a seamless and robust bond.

The fusion bonding process begins with the careful preparation of the silicon wafers. The surfaces that are to be bonded are meticulously cleaned and polished to ensure optimal bonding quality. Any contaminants or surface irregularities are removed to maximize the bonding interface's contact area and minimize defects.

Once the surfaces are prepared, the wafers are brought into close proximity and subjected to elevated temperatures and pressure. The temperature is precisely controlled to enable the atoms on the surface to diffuse and form bonds with the corresponding atoms on the other surface. The applied pressure helps in establishing intimate contact between the surfaces, ensuring efficient atomic-level bonding.

During the fusion bonding process, the silicon atoms rearrange themselves at the bonding interface, creating covalent bonds and resulting in a seamless integration between the two wafers. This bonding technique enables the formation of a strong, hermetic, and defect-free interface.

The benefits of fusion bonding include the absence of bonding agents or adhesives, which can introduce impurities, and the ability to achieve high bond strength and uniformity. Moreover, fusion bonding enables the creation of complex three-dimensional structures, precise alignment of device layers, and the integration of dissimilar materials, facilitating the development of advanced silicon-based devices and systems.

3a. Combine structure/process/material with correct process/material, e.g. A5, B6, … (0.5 points each). Unique solution exists, i.e. you cannot use same number or letter twice.

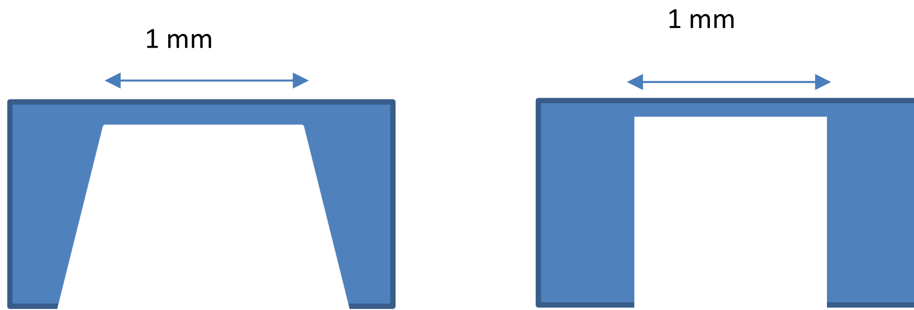
A) SOI 10 µm device layer etching	1) Cl_2 plasma
B) KOH thru-wafer etching	2) PR-masked DRIE
C) etching 1 µm LW Al lines	3) CF_4 plasma
D) etching nitride	4) RIE
E) etching 100 nm pitch grating	5) Si_3N_4 mask
F) 50 nm LW copper metallization	6) CMP

3b. Combine mask with process/structure. 0.5 points each. Unique solution exists, i.e. you cannot use same number or letter twice.

A) nitride mask	1) DRIE
B) oxide mask	2) KOH etch
C) photoresist mask	3) Cr on quartz
D) aluminum mask	4) LOCOS
E) no mask	5) 5 µm LW Al etch
F) photomask	6) spacer etch

4a) There are 50 mm^2 chips on 150 mm diameter wafer. The process is rated at one defect per square centimetre. A more advanced process is available that will allow a 30% linear shrink (LWs are 0.7×). But because it is a newer process and much denser, it is estimated to have defect density of five defects per square centimetre. What chip size in the new process will result in same yield as in the old one? (3p)

4b) MEMS sensor chip active area is 1*1 mm. It is fabricated on 500 µm thick, 200 mm diameter wafer. In the old version backside etching was done by KOH, but in the newer version by DRIE. How many chips fit on the wafer in these two versions? (3p)



5. Explain step-by-step the fabrication of this TFT. Give your estimates for device dimensions, film thicknesses, deposition methods etc. IGZO is Indium Gallium Zinc Oxide, a semiconductor that is deposited by reactive sputtering. 6 points.

6. Explain key fabrication issues in each step a-f. Note that some of them contain many main steps. Give details about the wafer dimensions, deposition methods, film thicknesses, linewidths etc. 6 points.