? Forums Quizzes Resources



Started on	Tuesday, 10 December 2024, 1:15 PM
State	Finished
Completed on	
Time taken	
Grade	18.50 out of 33.00 (56.06 %)

	Mark 0.50 out of 0.50	Correc
The magnitude of power gain in a two-port is said to change -3 dB. This change approximately of	corresponds to	
\bigcirc a. Reduction of 30 % of its original value		
 B. Reducing the gain to 1/2 of its original value 		
\bigcirc c. Reducing the gain to 1/4 of its original value		
Your answer is correct.		
The correct answer is:		
Reducing the gain to 1/2 of its original value		
uestion 2		
Ruestion 2	Mark 0.50 out of 0.50	Correc
A cylindrical conductor has DC resistance of 1 Ω . When is the resistance halved?	Mark 0.50 out of 0.50	Correc
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A cylindrical conductor has DC resistance of 1 Ω . When is the resistance halved?	Mark 0.50 out of 0.50	Correc
 a. When the length of the conductor is halved 	Mark 0.50 out of 0.50	Correc

The correct answer is: When the length of the conductor is halved

Question 3		
	Mark 0.50 out of 0.50	Correct
Norton equivalent is characterized as follows:		
$^{\odot}$ a. It has a current source in parallel with a resistor \checkmark		
O b. It has a current source equal to the current source of Thévenin equivalent		
\bigcirc c. It has a voltage source in series with a resistor		
Your answer is correct.		
The correct answer is:		
It has a current source in parallel with a resistor		

Question	4
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Mark 0.50 out of 0.50 Correct

Power transfer to load resistor $R_{
m L}$ from Thévenin equivalent with internal resistance of $R_{
m S}$ is maximized when

$$\bigcirc$$
 a. $R_{
m L} \ll R_{
m S}$
 \bigcirc b. $R_{
m L} \gg R_{
m S}$
 \bigcirc c. $R_{
m L} = R_{
m S}$ \checkmark

Your answer is correct.

The correct answer is: $R_{
m L}=R_{
m S}$

Question 5

Mark 0.50 out of 0.50 Correct

RMS value of 3.54 V corresponds to voltage

 \bigcirc a. $v=3.54\sin(2\pi ft)V$

- \odot b. $v=5\sin(2\pi ft+\Theta)V$ 🗸
- \bigcirc c. $v=12.5\sin(2\pi ft)V$

Your answer is correct.

The correct answer is: $v=5\sin(2\pi ft+\Theta)V$

Question 6		
	Mark 0.50 out of 0.50	Correct
A type of sensor has output impedance of 100 k Ω and its output voltage is amplified for digital re What should the input impedance of the amplifier be?	eadout without loading the	sensor.
\bigcirc a. The input impedance should be equal to the sensor output impedance		
\bigcirc b. The input impedance should be smaller than the sensor output impedance		
\odot c. The input impedance should be much larger than the sensor output impedance \checkmark		
Your answer is correct.		
The correct answer is:		
The input impedance should be much larger than the sensor output impedance		
Question 7		
	Mark 0.50 out of 0.50	Correct
An operational amplifier is characterized by equations: $v=v_+$, $i=0$, and $i_+=0$. Why are the	nese assumptions valid?	
 a. The output impedance is very small so the current to inputs is small 		
······································		
 b. The input terminals are virtually grounded, so there is equal voltage and zero currents c. The input impedance and gain of operational amplifier are very large 		
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 b. The input terminals are virtually grounded, so there is equal voltage and zero currents c. The input impedance and gain of operational amplifier are very large Your answer is correct. The correct answer is: The input impedance and gain of operational amplifier are very large Question 8	Mark 0.50 out of 0.50	Correct
 b. The input terminals are virtually grounded, so there is equal voltage and zero currents c. The input impedance and gain of operational amplifier are very large Your answer is correct. The correct answer is: The input impedance and gain of operational amplifier are very large	Mark 0.50 out of 0.50	Correct
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 b. The input terminals are virtually grounded, so there is equal voltage and zero currents c. The input impedance and gain of operational amplifier are very large Your answer is correct. The correct answer is: The input impedance and gain of operational amplifier are very large Ruestion 8 Voltage follower realized with an operational amplifier has a. Inverted output, because feedback is connected to inverting input b. Low input impedance, because the feedback has zero resistance and inputs are virtually s c. Non-inverted output, because the both inputs are at same potential 		Correct

Question 9		
	Mark 0.50 out of 0.50	Correct
Parallel-plate capacitor is charged to 1 C with a 5-V voltage source. After charging, the voltage source distance between the plates is doubled. What is the capacitor voltage after the change in plate distance between the plates is doubled.		, the
◎ a. 10 V ✓		
○ b. 5 V		
○ c. 2.5 V		
Your answer is correct.		
The correct answer is:		
10 V		
Question 10		
	Mark 0.00 out of 0.50	Incorrect
An air-filled coil has inductance of 1 μ H with 100 loops, how the inductance can be doubled?		
\bigcirc a. Reducing the diameter of the loops by about 41 %		
\odot b. Adding approximately 100 more loops 🗸		
C. Adding approximately 41 more loops		
Your answer is correct.		
The correct answer is: Adding approximately 100 more loops		
Question 11		
	Mark 0.50 out of 0.50	Correct
A port has voltage across it $ ilde{V}=0.6~{ m V}~{igstar}45^\circ$ and current $ ilde{I}=5~{ m mA}~{igstar}-45^\circ.$ What is the impedance	e seen across the port?	
\bigcirc a. $ ilde{Z}=120\Omega{ar ar 0^\circ}$		
\odot b. $ ilde{Z}=120\Omega{ar y}0^\circ{uckslash}$		

 \odot c. $ilde{Z}=120~\Omega$ $igstarrow -90^{\circ}$

Your answer is correct. The correct answer is:

 $ilde{Z}=120~\Omegaar{}{}^{2}90^{\circ}$

Small-signal conductance of a diode describes

- a. The conductance seen when the diode is reverse biased
- \odot b. Slope of the diode current versus its voltage at the bias point \checkmark
- O c. The leakage conductance parallel to the PN junction in the diode

Your answer is correct.

The correct answer is:

Slope of the diode current versus its voltage at the bias point

Question 13		
	Mark 0.50 out of 0.50	Correct
NMOS transistor is in saturation when		
\odot a. $V_{ m GS} > V_{ m T}$		
\odot b. $V_{ m DS} > V_{ m GS} - V_{ m T}$ 🗸		

 \odot c. $V_{
m DS} < V_{
m T}$

Your answer is correct.

The correct answer is: $V_{
m DS} > V_{
m GS} - V_{
m T}$

Question 14

Mark 0.50 out of 0.50 Correct

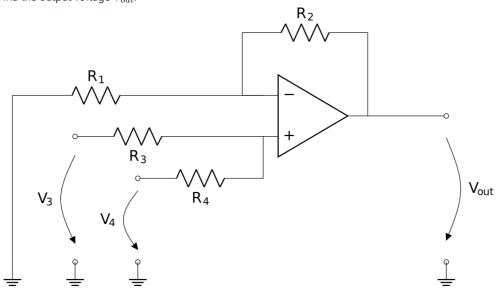
Channel-length modulation is modeled as

- \bigcirc a. Finite input impedance in transistor equivalent model
- \odot b. Finite output impedance in transistor equivalent circuit \checkmark
- O c. Reduction of transconductance in transistor equivalent model

Your answer is correct.

The correct answer is: Finite output impedance in transistor equivalent circuit



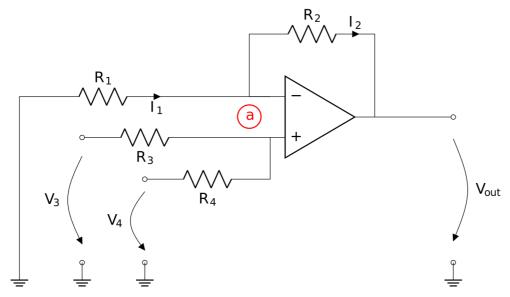


 $\begin{array}{ll} R_1 = 4 \ {\rm k}\Omega, & R_2 = 5 \ {\rm k}\Omega, & R_3 = 4 \ {\rm k}\Omega, & R_4 = 2 \ {\rm k}\Omega, & V_3 = 4 \ {\rm V}, & V_4 = 2 \ {\rm V} \\ V_{\rm out} = & \fbox{6} & {\rm V} \end{array}$

Your last answer was interpreted as follows:

1.5

The operational amplifier is assumed ideal so there is virtual short between the inputs and $V_{-}=V_{+}.$



The voltage at node a is then given with voltage division:

$$V_a = V_4 + rac{R_4}{R_3 + R_4} (V_3 - V_4)$$

The current through resistor R_1 is $I_1 = -v_a/R_1$. The current to inverting input is zero, so $I_2 = I_1$. The output voltage is $V_{out} = -(R_1 + R_2)I_1 = \frac{R_1 + R_2}{R_1}V_a$ $V_{out} = \frac{R_1 + R_2}{R_1}(V_4 + \frac{R_4}{R_3 + R_4}(V_3 - V_4))$ $V_{out} = \frac{R_1 + R_2}{R_1}(\frac{R_3}{R_3 + R_4}V_4 + \frac{R_4}{R_3 + R_4}V_3) = \frac{4 \text{ k}\Omega + 5 \text{ k}\Omega}{4 \text{ k}\Omega}(\frac{4 \text{ k}\Omega}{4 \text{ k}\Omega + 2 \text{ k}\Omega}2 \text{ V} + \frac{2 \text{ k}\Omega}{4 \text{ k}\Omega + 2 \text{ k}\Omega}4 \text{ V}) \approx 6 \text{ V}$

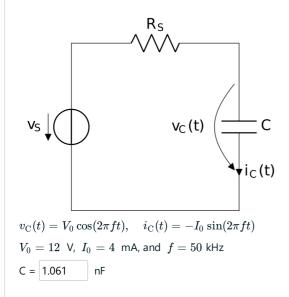
The answer 6, which can be typed as 6, would be correct.

Question 16

Mark 0.00 out of 4.00 Incorrect

The voltage $v_{\rm C}(t)$ across and current $i_{\rm C}(t)$ through a capacitor are shown in the figure below. What is the capacitance of the capacitor?

1

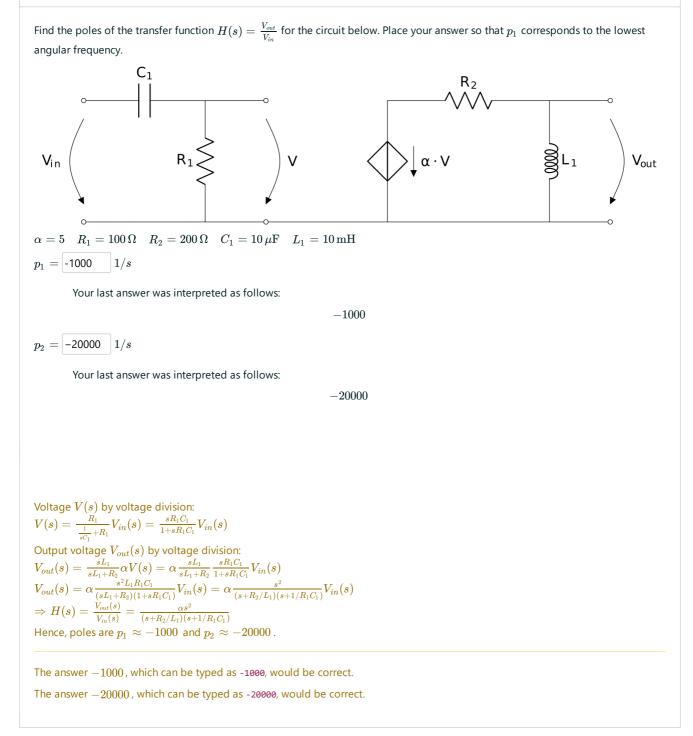


Your last answer was interpreted as follows:

For a capacitor $i_{
m C}(t)=Crac{dv(t)}{dt}$. Derivative of the voltage is: $rac{dv_{
m C}(t)}{dt}=-2\pi fV_0\sin(2\pi ft)$ Therefore, capacitance can be solved: $-I_0\sin(2\pi ft) = C(-2\pi fV_0\sin(2\pi ft))$ $-I_0=-2\pi f C V_0$ $C=rac{I_0}{2\pi f V_0}=rac{4~\mathrm{mA}}{2\pi imes 50~\mathrm{kHz} imes 12~\mathrm{V}}pprox rac{10}{3\cdot\pi}$ nF.

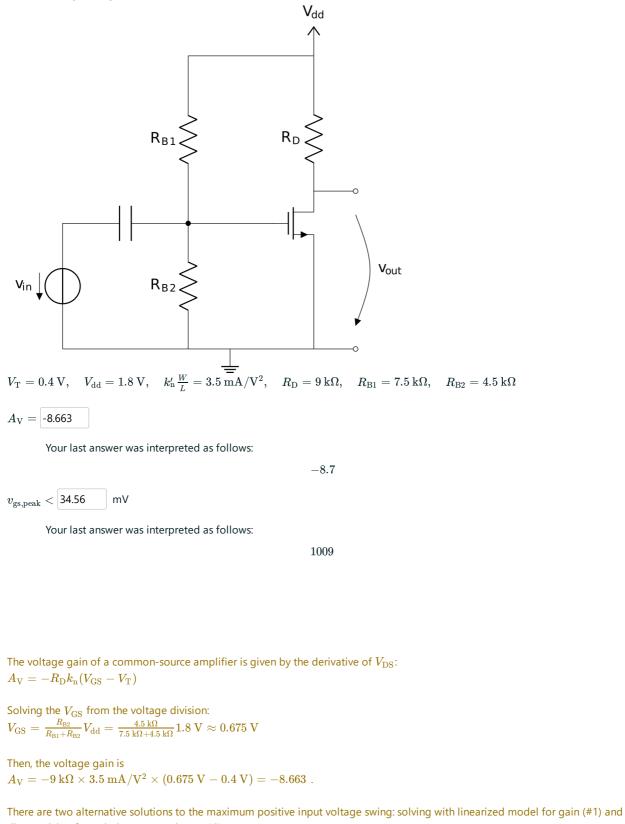
The answer 1.061, which can be typed as 1.061, would be correct.

Question 17



Question 18

Below is a common-source amplifier. Zero channel-length modulation is assumed. The capacitor C can be assumed to be a short circuit for the small-signal input voltage. What is the voltage gain for small input voltage? What is the maximum positive input voltage swing when the transistor still remains in saturation? Depending on approximations, two solutions for the maximum positive voltage swing exist.



direct solving from drain-source voltage (#2).

Solution #1:

The transistor is in saturation as long as $v_{
m DS} > v_{
m GS} - V_{
m T}$ (limit to triode, negative output swing, positive input swing). For positive input swing (capital letter represents DC bias point):

 $\begin{array}{l} v_{\mathrm{DS}} > v_{\mathrm{GS}} - V_{\mathrm{T}} \\ V_{\mathrm{DS}} - |A_{\mathrm{V}}| v_{\mathrm{gs}} > V_{\mathrm{GS}} + v_{\mathrm{gs}} - V_{\mathrm{T}} \\ v_{\mathrm{gs}} < \frac{V_{\mathrm{DS}} - V_{\mathrm{GS}} + V_{\mathrm{T}}}{1 + |A_{\mathrm{V}}|} \end{array}$

The drain-source voltage at the bias point is: $V_{\rm DS} = V_{\rm dd} - \frac{R_{\rm D}}{2} k'_{\rm n} \frac{W}{L} (V_{\rm GS} - V_{\rm T})^2$ $V_{\rm DS} = 1.8 \text{ V} - \frac{9 \text{ k}\Omega}{2} \times 3.5 \text{ mA}/\text{V}^2 \times (0.675 \text{ V} - 0.4 \text{ V})^2 = 0.6089 \text{ V}$

At positive input signal just exceeding the limit, $v_{\rm gs} = v_{\rm gs,peak}$: $v_{\rm gs,peak} = \frac{V_{\rm Ds} - V_{\rm GS} + V_{\rm T}}{1 + |A_{\rm V}|} = \frac{0.6089 \, {\rm V} - 0.675 \, {\rm V} + 0.4 \, {\rm V}}{1 + |-8.663|} \approx 34.56 \, {\rm mV}.$

Solution #2:

The drain-source voltage at the threshold of going to triode mode is $v_{\rm DS} = v_{\rm GS} - V_{\rm T}$. Then, writing the drain-source voltage with help of gate-source and threshold voltages, supply voltage and drain resistor, we get:

$$\begin{split} V_{\rm DS} &= V_{\rm dd} - \frac{R_{\rm D}}{2} k_{\rm n} (V_{\rm GS} - V_{\rm T})^2 \\ V_{\rm GS} - V_{\rm T} &= V_{\rm dd} - \frac{R_{\rm D}}{2} k_{\rm n} (V_{\rm GS} - V_{\rm T})^2 \\ V_{\rm GS} - V_{\rm T} &= V_{\rm dd} - \frac{R_{\rm D}}{2} k_{\rm n} (V_{\rm GS}^2 - 2V_{\rm T} V_{\rm GS} + V_{\rm T}^2) \\ \\ \frac{R_{\rm D}}{2} k_{\rm n} V_{\rm GS}^2 + (1 - R_{\rm D} k_{\rm n} V_{\rm T}) V_{\rm GS} + \frac{R_{\rm D}}{2} k_{\rm n} V_{\rm T}^2 - V_{\rm T} - V_{\rm dd} = 0 \end{split}$$

The gate-source voltage is second order polynomial. In addition to the DC bias there is positive input voltage swing (

$$\begin{split} v_{\rm GS} &= V_{\rm GS} + v_{\rm gs,pos,peak});\\ v_{\rm GS} &= \frac{-b\pm\sqrt{b^2-4ac}}{2a}\\ a &= \frac{R_{\rm D}}{2}k_{\rm n}\\ b &= 1 - R_{\rm D}k_{\rm n}V_{\rm T}\\ b^2 &= 1 - 2R_{\rm D}k_{\rm n}V_{\rm T} + R_{\rm D}^2k_{\rm n}^2V_{\rm T}^2\\ c &= \frac{R_{\rm D}}{2}k_{\rm n}V_{\rm T}^2 - V_{\rm T} - V_{\rm dd}\\ v_{\rm GS} &= \frac{R_{\rm D}k_{\rm n}V_{\rm T}^{-1\pm\sqrt{1-2R_{\rm D}k_{\rm n}V_{\rm T} + R_{\rm D}^2k_{\rm n}^2V_{\rm T}^2 - 4\frac{R_{\rm D}}{2}k_{\rm n}(\frac{R_{\rm D}}{2}k_{\rm n}V_{\rm T}^2 - V_{\rm T} - V_{\rm dd})}{\frac{2\frac{R_{\rm D}}{2}k_{\rm n}}{v_{\rm GS} + V_{\rm T}} + \frac{\pm\sqrt{1-2R_{\rm D}k_{\rm n}V_{\rm T} + R_{\rm D}^2k_{\rm n}^2V_{\rm T}^2 - R_{\rm D}^2k_{\rm n}^2V_{\rm T}^2 + 2R_{\rm D}k_{\rm n}(V_{\rm T} + V_{\rm dd}) - 1}{R_{\rm D}k_{\rm n}}}\\ v_{\rm GS} &= V_{\rm T} + \frac{\pm\sqrt{1-2R_{\rm D}k_{\rm n}V_{\rm T} + R_{\rm D}^2k_{\rm n}^2V_{\rm T}^2 - R_{\rm D}^2k_{\rm n}^2V_{\rm T}^2 + 2R_{\rm D}k_{\rm n}(V_{\rm T} + V_{\rm dd}) - 1}{R_{\rm D}k_{\rm n}}} \end{split}$$

Clearly, the solution + is correct, since the gate-source voltage needs to be larger than the threshold voltage. Finally, writing with bias V_{GS} and input voltage $v_{\text{gs,pos,peak}}$:

$$egin{aligned} v_{
m gs,pos.peak} &= V_{
m T} - V_{
m GS} + rac{\sqrt{1+2R_{
m D}k_{
m n}V_{
m dd}-1}}{R_{
m D}k_{
m n}} \ v_{
m gs,pos.peak} &= 0.4 \ {
m V} - 0.675 \ {
m V} + rac{\sqrt{1+2 imes 9 \ {
m k}\Omega imes 3.5 \ {
m mA}/{
m V}^2 imes 1.8 \ {
m V}-1}}{9 \ {
m k}\Omega imes 3.5 \ {
m mA}/{
m V}^2} pprox 32.8 \ {
m mV}. \end{aligned}$$

The solution with linearized model and gain gives slightly larger value as it does not consider the nonlinearity. Directly solving from drain-source voltage gives more realistic value for the maximum input signal. Both solutions are considered correct in the exam.

Voltage gain is $A_{\rm V} \approx -8.663$ and maximum positive swing in input voltage (maximum negative swing in output) is $v_{\rm gs,peak} < 34.56$ mV or $v_{\rm gs,peak} < 32.8$ mV.

The answer -8.663, which can be typed as -8.663, would be correct.

The answer 34.56, which can be typed as 34.56, would be correct.

Previous activity

Exercise 12: Deadline on December 2