S-87.3190 Computer Architecture (5 cr)
Exam 14.5.2007
Please write clearly. Voit myös vastata suomeksi.

1a) With A (=F) and B (=2) and SUM = A + B. What is SUM (in Hexadecimal) if all three variables (A, B, SUM) are represented with 4 bits and:

- sign magnitude?
- ones complement?
- unsigned?
- twos complement?
- encoded with a bias of 7 (as the exponent is encoded in floating point). (7p)

b) Was there overflow in any of the cases in a)? (1p)

c) IBM just unveiled the Power6 dual-core RISC architecture. Compared to equivalent RISC and x86 implementations, what is a superior feature in the Power6? (1p)

d) AMD just revealed the Opteron quad-core architecture. Compared to Intel's current quad-core implementations, what is special about the implementation of the quad-core Opteron? (1p)

2. MIPS has the following instruction stages: Ifetch, Decode, Execute, Memory, Write Back.

a) By using these stages, explain the concept of Pipelining (2p)

b) What is the main advantage of pipelining (1p)

c) Given the following MIPS code snippet (note that instruction #6 could be anything). Insert no-ops to insure correct operation. *Assume no delayed branch, no forwarding units and no interlocked pipeline stages.* (7p)

```
loop:
1 addi $t0, $t0, 4
2 lw $v0, 0($t0)
3 sw $v0, 20($t0)
4 lw $s0, 60($t0)
5 bne $s0, $0, loop
6                ## ← The following instruction could be anything!
```

3 Suppose we have a 16KiB (1 KiB = 1024B) of data in a direct-mapped cache with 4 word (word = 32 bits) blocks. Show what happens in the cache when the addresses below are read from memory. The memory values are shown on the right.

```
1.0x00000014
2.0x00000034
3.0x00008014
4.0x0000801C
```

=> TURN OVER

Memory

Address (hex)	Value of Word
...	...
00000010	a
00000014	b
00000018	c
0000001C	d
...	...
00000030	e
00000034	f
00000038	g
0000003C	h
...	...
00008010	i
00008014	j
00008018	k
0000801C	l

4. For the two MIPS instructions shown below (instruction format also shown):

ADDU (Add Unsigned)

op	rs	rt	rd	shamt	funct
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

ADDI (Add Immediate)

op	rs	rt	Immediate
6 bits	5 bits	5 bits	16 bits

a) Explain the meaning of the instruction fields (3p)

b) Construct a single-cycle 32-bit datapath which can implement the two instructions (include bit-widths, explain control signals) (7p)