S-87.3190 Computer Architecture (5 cr)
Exam 30.8.2006
Please write clearly. Voit myös vastata suomeksi.

1. Suppose we have a 2's complement fixed-point 4-bit number representation with three fractional bits, as follows: *b3.b2b1b0* (note, the binary point is to the right of the most significant bit). For each of the following values, write down the closest possible (most accurate) 4-bit fixed-point number representation. (3p)

a) 1/3
b) −3/4
c) 1.0_{ten}
d) Explain the meaning of an Instruction Set Architecture (ISA). Also explain what is included in an ISA (5p)
e) To achieve more processing power in the near future, will state-of-the-art general processors move towards 1) higher clock speeds and single-core designs, or 2) multi-core designs with proportionally lower clock speeds? Explain briefly why (2p)

2a) Implement the following pseudo-instruction loop with MIPS instructions: (6p)

```
Loop:   g = g + A[i];
        i = i + j;
        if (i = h) goto Loop;
        # g: $s1, h: $s2, i: $s3, j: $s4, $s5:base address of A
```

b) Show the instruction format and explain the meaning of the instruction fields for the MIPS instruction `ADDU`. (4p)

3a) Explain the concept of forwarding. For what purpose and how is forwarding used in MIPS. (2p)
b) What is done when forwarding is not a solution? (1p)
c) What type of memory technology is used in the following memory levels: Register, cache, computer main memory, disc. Explain. (4p)
d) Explain briefly the meaning of a direct mapped cache. (3p)

4. Construct a single-cycle 32-bit datapath which can implement the two MIPS instructions `ADDU`, `ADDI` (include bit-widths, explain control signals) (10p)