S-87.3190 Computer Architecture (5 cr) Exam 11.5.2009

Please write clearly. **Voit myös vastata suomeksi.**

Mark your project completion year / Merkitse harjoitustyön suorittamisvuosi

1. a) Assuming the stick-man in Fig. 1 is controlled by a MIPS CPU, what goes wrong in the third panel? (2p)
   b) How could the problem in panel three be avoided? (2p)
   c) Explain the major differences between a general purpose CPU (such as MIPS) and a DSP processor. (4p)
   d) Give a short example on where Thread Level Parallelism can be found. (2p)

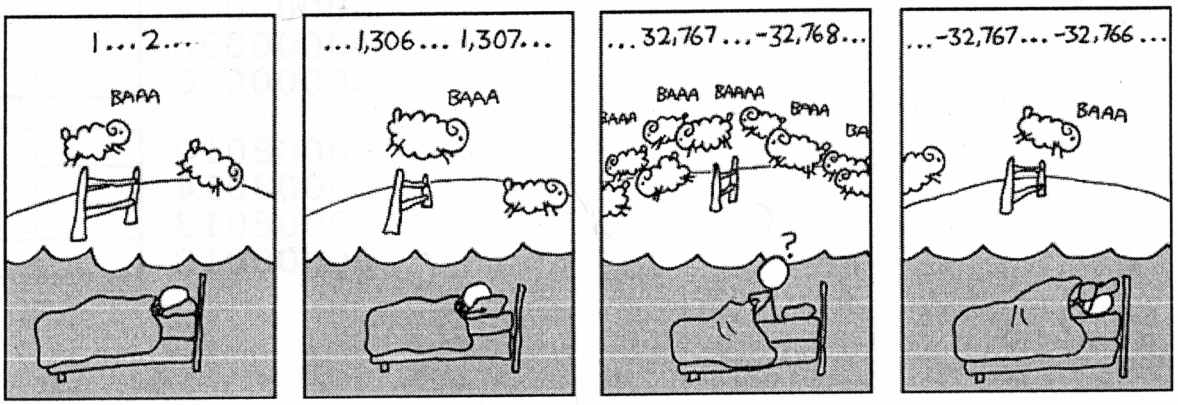

Fig. 1

2. a) Prior to the early 1980s, machines were built with more and more complex instruction set. The MIPS is a RISC machine. Why has there been a move to RISC machines away from complex instruction machines? (3p)
   b) In MIPS assembly, write an assembly language version of the following C code segment:

```
int A[100], B[100];
for (i=1; i < 100; i++) {
A[i] = A[i-1] + B[i];
}
```

   At the beginning of this code segment, the only values in registers are the base address of arrays A and B in registers $a0 and $a1. (7p)

3. a) Explain the concept of Pipelining (2p)
   b) What does the concept forwarding mean? What for and how is it used in MIPS? What can be done when forwarding does not solve a problem? (3p)
   c) Add the necessary hardware to the pipeline of Fig. 2 to enable forwarding. (5p)

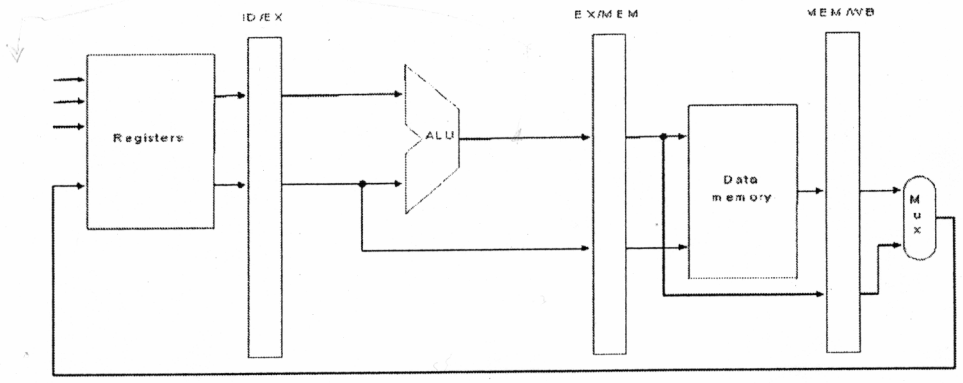

Fig. 2

TURN OVER =>

4. Suppose we have a 16KiB (1 KiB = 1024B) of data in a direct-mapped cache with 4 word (word = 32 bits) blocks. Show what happens in the cache when the addresses below are read from memory. The memory values are shown on the right.

   1. 0x00000014
   2. 0x00000034
   3. 0x00008014
   4. 0x0000801C

Memory

Address (hex)	Value of Word
...	...
00000010	a
00000014	b
00000018	c
0000001C	d
...	...
00000030	e
00000034	f
00000038	g
0000003C	h
...	...
00008010	i
00008014	j
00008018	k
0000801C	l