S-87.3190 Computer Architecture (5 cr) Exam 7.1.2010

Please write clearly. **Voit myös vastata suomeksi.**

Mark your project completion year / Merkitse harjoitustyön suorittamisvuosi

1. Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 80 MHz and M2 has a clock rate of 100 MHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows:

Instruction Class	Machine M1 – Cycles/Instruction Class	Machine M2 – Cycles/Instruction Class	Frequency
A	1	2	60%
B	2	3	30%
C	4	4	10%

a) Calculate the average CPI for each machine, M1, and M2.
b) Calculate the average MIPS ratings for each machine, M1 and M2.
c) Which machine has a smaller MIPS rating ? Which individual instruction class CPI do you need to change, and by how much, to have this machine have the same or better performance as the machine with the higher MIPS rating (you can only change the CPI for one of the instruction classes on the slower machine)?
d) Explain the concept of Pipelining.

2. Consider a processor with the following specification:
   - Standard five (5) stage (F, D, E, M, W) pipeline.
   - No forwarding.
   - Stalls on all data and control hazards.
   - Non-delayed branches
   - Branch comparison occurs during the second stage.
   - Instructions are not fetched until branch comparison is done.
   - Memory CAN be read/written on same clock cycle.
   - The same register CAN be read & written on the same clock cycle.

```
add $t1, $t2, $t3
xor $t1, $t4, $t5
lw $t3, 0($t1)
beq $t3, $t3, 1
lw $t5, 0($t3)
xor $t4, $t5, $t6
add $t5, $t5, $t4
```

a) Count how many cycles will be needed to execute the code on the right and write out each instruction's progress through the pipeline by filling in the table below with pipeline stages (F, D, E, M, W).

Cycle →	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
Inst 1	F																								
Inst 2																									
Inst 3																									
Inst 4																									
Inst 5																									
Inst 6																									
Inst 7																									

TURN OVER =>

b) In the MIPS assembler code on the right, how many times is instruction memory accessed? How many times is data memory accessed? (Count only accesses to memory, not registers.)

```
lw $v1, 0($a0)
addi $v0, $v0, 1
sw $v1, 0($a1)
addi $a0, $a0, 1
```

3. a) Describe the operation of a set-associative cache. Compare it to other types of caches.
b) Design a 128KB direct-mapped data cache that uses a 32-bit address and 16 bytes per block. Calculate the following: (1) How many bits are used for the byte offset? (2) How many bits are used for the set (index) field? (3) How many bits are used for the tag?
c) Design a 8-way set associative cache that has 16 blocks and 32 bytes per block. Assume a 32 bit address. Calculate the following: (1) How many bits are used for the byte offset? (2) How many bits are used for the set (index) field? (3) How many bits are used for the tag?
d) Why is miss rate not a good metric for evaluating cache performance? What is the appropriate metric? Give its definition.
e) What is the reason for using a combination of first and second- level caches rather than using a larger first-level cache?

4a) Below is the single-cycle MIPS datapath presented during lecture. Your job is to modify the diagram for multicycle operation (7p)
b) Also explain how the control changes with multi-cycle operation (3p)