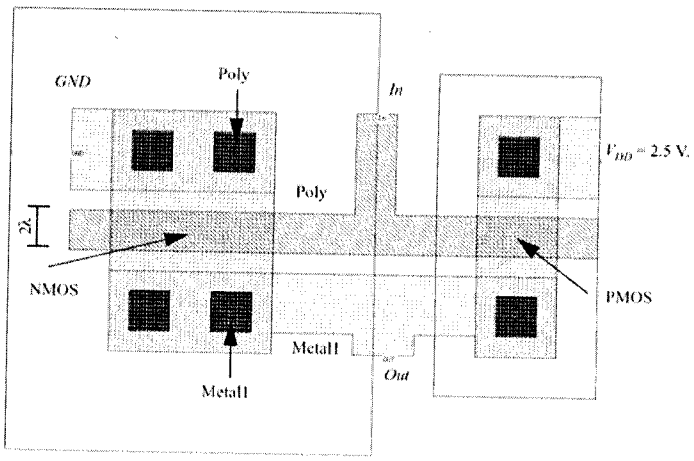
S-87.3182 Digital microelectronics I: System level electric design (5 cr)
Exam 14.12.2009. Please write clearly. Voit vastata myös **suomeksi**

1) a) The layout of a static CMOS inverter is given on the right. (λ = 0.125 μm). Determine the sizes of the NMOS and PMOS transistors. (1p)



b) Approximate the VTC of the inverter and derive its parameters (VOH, VOL, VM, VIH, and VIL). VDD=2.5V and assume that $k_p V_{DSATp} = k_n V_{DSATn}$ (4p)

c) Is the VTC affected when the output of the gates is connected to the inputs of 4 similar gates? (1p)

d) Approximately resize the inverter to achieve a switching threshold of approximately 0.75 V. Do not layout the new inverter. How are the noise margins affected by this modification? (4p)

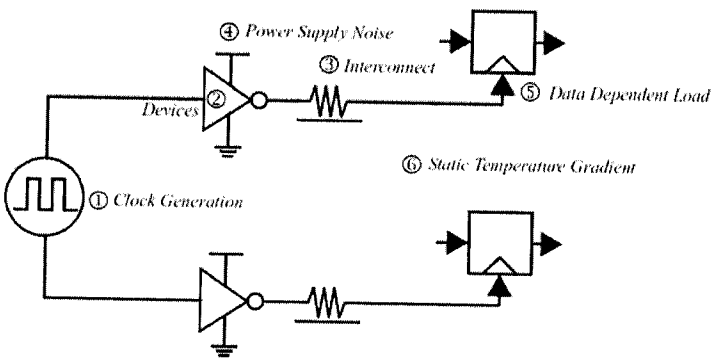
2) Consider scaling a CMOS technology by S > 1. In order to maintain compatibility with existing system components, you decide to use constant voltage scaling.

a) In traditional constant voltage scaling, transistor widths scale inversely with S, W∝1/S. To avoid the power increases associated with constant voltage scaling, however, you decide to change the scaling factor for W. What should this new scaling factor be to maintain approximately constant power. Assume long-channel devices (i.e., neglect velocity saturation). (5p)

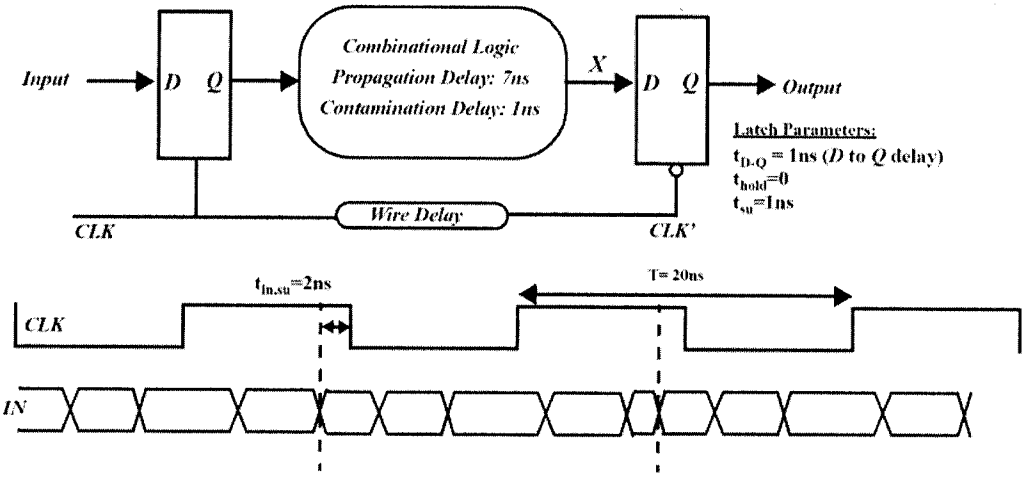
b) How does delay scale under this new methodology? (2p)

c) For a technology scaling factor of s = 0.5, derive the relationship between gate delay and semi-global wire delay. Both the wire width and height scale by s and the capacitance of a semi-global wire can be thought of as a constant. (3p)

3) a) A balanced clock distribution scheme is shown on the right. Explain each source of variation and identify whether it contributes to skew or jitter. (4p)



b) Consider the following latch based pipeline circuit shown below. Assume that the input, IN, is valid (i.e., set up) 2ns before the falling edge of CLK and is held till the falling edge of CLK (there is no guarantee on the value of IN at other times). Determine the maximum positive and negative skew on CLK' for correct functionality. (You can assume that $t_{C\text{-}Q}$ is also 1ns.) (6p)



4) a) Draw the schematic of the 3-input NAND gate, and size all transistors such that the worst-case delay is equal to that of a minimum sized 2/1 inverter. (4p)
b) Find the logical effort (g) of the 3-input NAND gate. (1p)
c) For the logic path from node (A) to node (B) shown in the figure below, find the path branching effort, path electrical effort, path logical effort, and total path effort. What is the optimum effort per stage for minimizing delay? (6p)