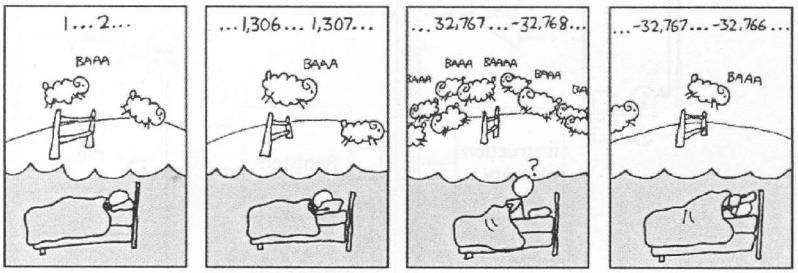
S-87.3190 Computer Architecture (5 cr) Exam 14.5.2010

Please write clearly. **Voit myös vastata suomeksi.**

Mark your project completion year / Merkitse harjoitustyön suorittamisvuosi

1. a) Assuming the stick-man on the right is controlled by a MIPS CPU, what goes wrong in the third panel? (1p)



b) How could the problem in panel three be avoided? (1p)

c) A processor run on a particular benchmark has the instruction mix and CPI shown in the table at the right. *How many times faster* would the benchmark run if we quadruple the CPI of the ALU from 2 to 8? (2p)

	Frequency	CPI
Memory	30%	4
Branch	20%	4
ALU	50%	2 → 8

d) What's the speedup (over a 1-core machine) for a 20%-serial program on a 16-core machine? (2p)

e) Which is the best way to communicate with a remote sensor measuring lunar eclipses (kuunpimennys), via polling or interrupts (please explain)? (1p)

f) Consider two competing floating-point formats below. Each contains the same fields (sign, exponent, significand) and follows the same general rules as the 32-bit IEEE standard (denorms, biased exponent, non-numeric values, etc.), but allocates bits differently. Calculate the exponent bias, denorm implicit exponent, and number of NANs for both formats. (3p)

Implementation "LEFT"

S	EE	FF

Implementation "RIGHT"

S	EEE	F

2. a) Instead of using a special hardware multiplier, it is possible to multiply using shift and add instructions. This is particularly attractive when multiplying by small constants. Suppose we want to put nine times the value of `$s0` into `$s1`, ignoring any overflow that may occur. Show a minimal sequence of MIPS instructions for doing this without using a multiply instruction. (4p)

b) Explain the operation of a direct-mapped cache. (2p)

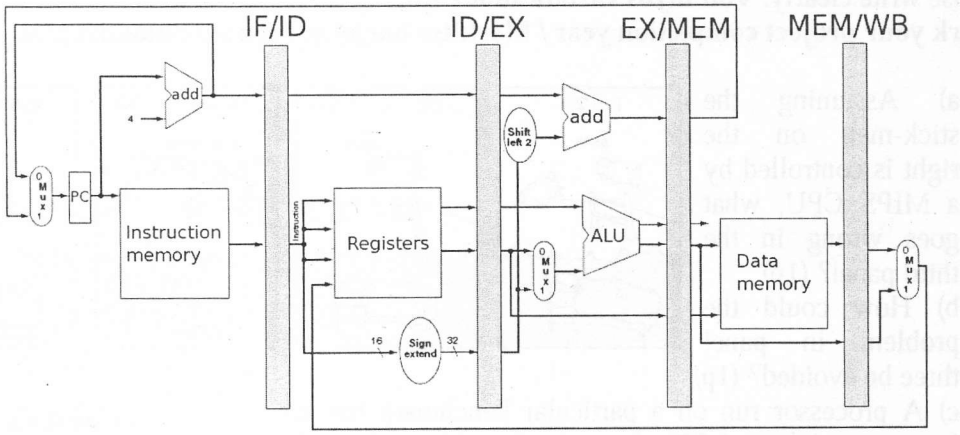
c) For a direct-mapped cache design with a 32-bit address, 64 entries, and a block size of 4 (in words), starting from power on, the byte-addressed cache references below are recorded. For each address show whether there is a cache hit or miss and whether the block is replaced. Also calculate the total hit ratio. (4p)

Address	0	4	16	132	232	160	1024	30	140	3100	180	2180

3. a) Explain the concept of pipelining (2p)

TURN OVER =>

b) Shown below is a simple diagram of the pipelined datapath. Explain what needs to added to the datapath to allow correct control of the datapath. (You do not have to draw the control signals, but explain the changes in general terms, drawings, etc.) (3p)



b) Explain how multiple instructions are issued in a single clock cycle in WLIV and superscalar CPUs (3p)

c) Explain the main differences between a CPU and a GPU (2p)

4. Modify the following single cycle MIPS datapath diagram to accommodate a new instruction `swai` (store word then auto-increment). The operation performs the regular `sw` operation, then post-increments the `rs` register by 1. Your modification may use simple adders, mux chips, wires, and new control signals. You may replace original labels where necessary. Recall the RTL for `sw` is:
`Mem[R[rs] + SignExt[imm16]] = R[rt]; PC=PC+4`, & that `sw` (and `swai`) has the following fields:

Opcode	Rs	Rt	Immediate

a) Modify the picture below and draw (or list) your changes below (you may draw or list on the exam paper or draw on the figure below). (7p)

b) We also wish to do the same thing with `lw`, namely create `lwai`. Will this work (please explain)? (3p)