S-87.3190 Computer Architecture (5 cr) Exam 25.5.2011

Please write clearly. Voit myös vastata suomeksi.

Mark your project completion year / Merkitse harjoitustyön suorittamisvuosi

A calculator is not allowed

1. a) Explain what is included in an Instruction Set Architecture (3p)
   b) Explain the concept of Memory Mapped I/O. (2p)
   c) Explain the concept of program threads. (2p)
   d) Explain the concept of Cache Coherence. (3p)

2. Compile the following code snippet into MIPS assemby code (the snippet is part of larger code and meaningless by itself). `var` is stored in `$t0`, `i` is stored in `$t1`, and the pointer `ptr` is in `$t2`. Ignore register conventions for this problem. You must comment your code! Do not use mult!

```
// var and i are signed integers
// ptr is a pointer (a memory address) to a sufficiently large
// array of integers
i = 0;
while (var != 0) {
      var = var * 2;
      i++;
}
if (i >= 0) {
      var = *ptr; // assign the content in mem address ptr to var
}
else {
      var = *(ptr+i);
}
```

3. a) Describe the operation of a set-associative cache. Compare it to other types of caches. (2p)
   b) Design a 128KB direct-mapped data cache that uses a 32-bit address and 16 bytes per block. Calculate the following: (1) How many bits are used for the byte offset? (2) How many bits are used for the set (index) field? (3) How many bits are used for the tag? (2p)
   c) Design an 8-way set associative cache that has 16 blocks and 32 bytes per block. Assume a 32 bit address. Calculate the following: (1) How many bits are used for the byte offset? (2) How many bits are used for the set (index) field? (3) How many bits are used for the tag? (2p)
   d) Why is miss rate not a good metric for evaluating cache performance? What is the appropriate metric? Give its definition. (2p)
   e) What is the reason for using a combination of first and second- level caches rather than using a larger first-level cache? (2p)

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4. Below is the single-cycle MIPS datapath you all know and love. Ignore pipelining for the question. Your job is to modify the diagram to support a new MIPS instruction to perform the following pseudo code in one instruction (`ptr` is an array of integers in memory):

```
if(ptr[IMMEDIATE] == 0) then
ptr[IMMEDIATE] = 1;
```

We'll call our new instruction `soiflz`, for `store one if load zero`. If the word (that is stored `IMMEDIATE` integers past the base pointer in `rs`) is 0, then set that word to be 1.

a) Make up the syntax for the `soiflz` MIPS instruction (show an example where `ptr` is in register `$t0`, and IMMEDIATE is 8). Also show the register transfer language (RTL) description of `soiflz`. (4p)
b) Is it possible to implement this instruction in a single cycle datapath? If yes, modify the datapath below (you can draw your changes right in the figure) to enable `soiflz` and list all changes. Your modification may use adders, shifters, muxes, wires, and new control signals. If necessary, you may replace existing labels. If not possible, show why not. (5p)
c) What problems this instruction would cause in a pipelined datapath? (1p)