S-87.3190 Computer Architecture (5 cr) Exam 3.1.2012 Please write clearly. Voit myös vastata suomeksi. Mark your project completion year / Merkitse harjoitustyön suorittamisvuosi

A calculator is not allowed

1. a) Explain the meaning of an Instruction Set Architecture (3p)

/10p

- b) Explain the concept of program threads. (2p)
- c) Why are threads important in GPU systems. (1p)
- d) What is the meaning of N = 0b1101 if it is interpreted as a: (4p)
  - Sign/Magnitude number (write your answer in decimal);
  - Twos Complement number (write your answer in decimal);
  - Unsigned number (write your answer in decimal);
  - Float with SEEM format (1 Sign (S) bit, 2 Exponent (E) bits, 1 Significant (M) bit, bias = 1)
- 2. a) Explain the three MIPS instruction formats. (5p)
  - b) The following MIPS instructions that are listed below are located at the memory location 0x70000008. Assume \$t0 contains 0xDEADBEEF. What is the address of the next instruction that will be executed in each case? (5p) 000010 11111 11100 00000 00000 000011 (= j instruction) 000000 01000 00000 00000 001000 (= jr \$t0) 000101 01000 00000 11111 11111 111110 (= bne \$t0 \$zero offset=-210)

000101 01000 00000 11111 11111 111110 (= bne \$t0, \$zero, offset=-2<sub>10</sub>) 000000 00000 01000 01000 00000 100011 (= subu \$t0, \$zero, \$t0)

3. Consider a variation on the canonical MIPS 5 stage pipeline, which doesn't have any bypass paths, doesn't have branch delay slots, and resolves branches in the execute stage. For the following code sequence, answer all questions (2p each)

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/10 p

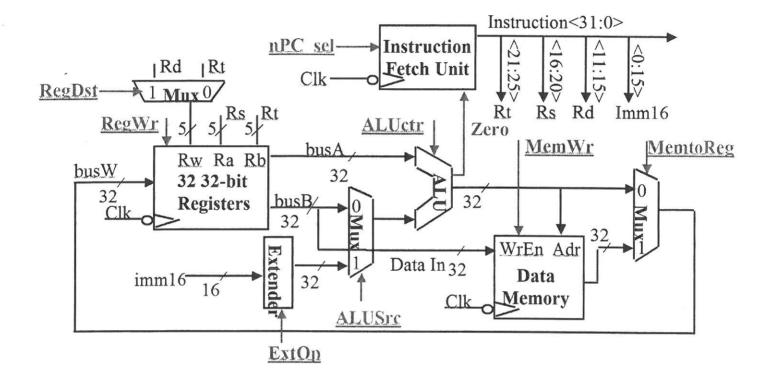
```
addu $t3, $t4, $t5
beq $t0, $t1, label
srlv $s0, $s1, $s2
addu $t4, $t4, $t4
```

- a) When \$t0 != \$t1, how many instruction fetches are wasted in the original processor?
- b) When \$t0 == \$t1, how many instruction fetches are wasted in the original processor?
- c) Assume the branches are resolved in the decode stage. When \$t0 == \$t1, how many instruction fetches are wasted?
- d) Assume the processor implements branch delay slots, and branches are resolved in the decode stage. Reorganize the code sequence to minimize number of wasted instruction fetches when \$t0 == \$t1.
- Given the code sequence in (g), how many instruction fetches are wasted when t0 = t1?

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- 4. a) Explain how virtual memory functions. (4p)
  - b) Below is the single-cycle MIPS datapath presented during lecture. Your job is to modify the diagram for multicycle operation (4p)
  - c) Also explain how the control changes with multi-cycle operation (2p)



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