TENTTI 27.10.2011

- 1. Are the following statements true (T) or false (F)? Every correct answer gives you +1 p and every wrong one -1 p. An empty answer is worth 0 p.
 - a) Moore's law became invalid about 7 years ago when the growth of clock frequencies of high-performance processors practically stopped.
 - b) Processor's instruction pipeline introduces statistical variation to the instruction execution times.
 - c) A DPRAM chip can be used conveniently for connecting two processors together.
 - d) It is never practical to disable interrupts in an embedded system.
 - e) Vectored interrupt is the most efficient way to interface a processor to a fast communications bus that transfers large data blocks.
 - f) The use of 8-bit processors in embedded systems will decrease significantly during the ongoing decade.
- 2. a) What are the so-called phantom interrupts, and how the software designer of an embedded system can minimize their effects?
 - b) An embedded system has multiple possible sources of interrupt. What kinds of procedures are used when more than one interrupt request is activated simultaneously? (Or which interrupt will be serviced first?)
- Explain the fundamental characteristics of processor's superscalar architecture and judge its advantages and disadvantages in time-critical real-time systems.
- 4. You are designing a user interface for a frequency converter and end up using a keypad with 16 keys. You have available a microcontroller with only 8 separate I/O lines of which every line can be programmed as an input or output. Draw a block diagram of the keypad interface to the microcontroller and explain with its help the operational sequence of monitoring the keypad status and identifying a possible single key pressure.
- 5. Your embedded system has an 8-bit microprocessor, which has a 16-bit address bus. In addition, you have a 32-Kbyte FLASH chip, a 16-Kbyte SRAM chip, and a 16-Kbyte DPRAM chip. You want to locate the FLASH chip right in the beginning of the address space, the SRAM chip just after it, and the DPRAM at the end of the address space. All the memory chips have a single /CS selection line, which is controlled by a fast 8 x 4 OTP-ROM chip. What are you going to program into the contents of the OTP-ROM, and how do you connect it to the microprocessor and the memory chips?