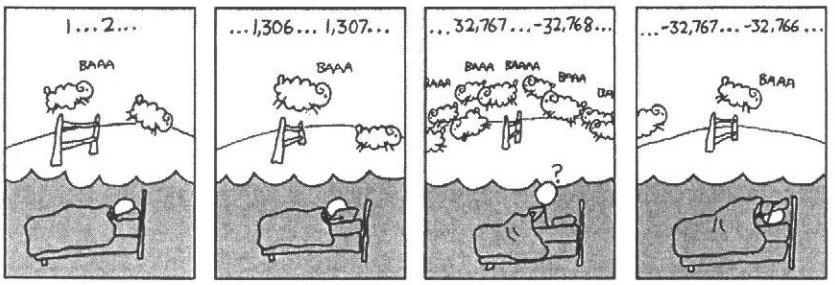
S-87.3190 Computer Architecture (5 cr) Exam 28.10.2011

Please write clearly. Voit myös vastata suomeksi.

Mark your project completion year / Merkitse harjoitustyön suorittamisvuosi

A calculator is not allowed

1. a) Assuming the stick-man on the right is controlled by a MIPS CPU, what goes wrong in the third panel? (1p)
b) How could the problem in panel three be avoided? (1p)



c) A processor run on a particular benchmark has the instruction mix and CPI shown in the table at the right. *How many times faster* would the benchmark run if we quadruple the CPI of the ALU from 2 to 8? (2p)

	Frequency	CPI
Memory	30%	4
Branch	20%	4
ALU	50%	2 → 8

d) What's the speedup (over a 1-core machine) for a 20%-serial program on a 16-core machine? (2p)

e) Which is the best way to communicate with a remote sensor measuring lunar eclipses (kuunpimennys), via polling or interrupts (please explain)? (1p)

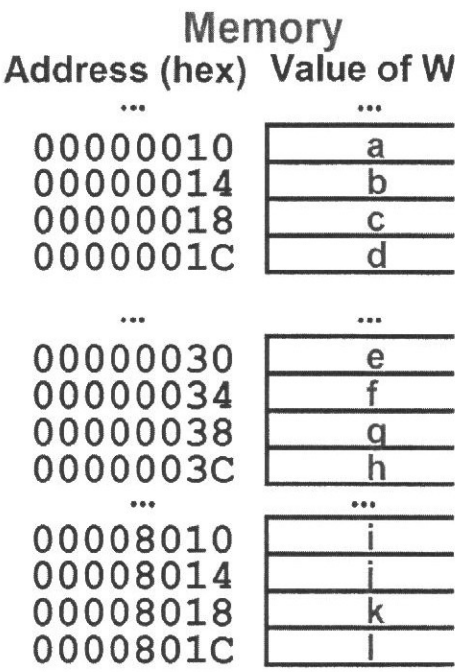
f) Consider two competing floating-point formats below. Each contains the same fields (sign, exponent, significand) and follows the same general rules as the 32-bit IEEE standard (denorms, biased exponent, non-numeric values, etc.), but allocates bits differently. Calculate the exponent bias, denorm implicit exponent, and number of NANs for both formats. (3p)

Implementation "LEFT"

Implementation "RIGHT"

2. Suppose we have a 16KiB (1 KiB = 1024B) of data in a direct-mapped cache with 4 word (word = 32 bits) blocks. Show what happens in the cache when the addresses below are read from memory. The memory values are shown on the right.

```
1. 0x00000014
2. 0x00000034
3. 0x00008014
4. 0x0000801C
```



TURN OVER =>

3. Consider a variation on the canonical MIPS 5 stage pipeline, which doesn't have any bypass paths, doesn't have branch delay slots, and resolves branches in the execute stage. For the following code sequence, answer questions (a) - (c).

```
addu $t0, $a0, $a1
sllv $t1, $t0, $a2
```

a) How many cycles does the processor stall (2p)?

b) Assume we have added a forwarding path from the beginning of the writeback stage to the beginning of the execute stage. How many cycles does the processor stall (2p)?

c) Assume we have implemented all forwarding paths. How many cycles does the processor stall (2p)?

For the following code sequence, answer questions (d)-(e).

```
addu $t3, $t4, $t5
beq $t0, $t1, label
srlv $s0, $s1, $s2
addu $t4, $t4, $t4
```

d) When $t0 != $t1, how many instruction fetches are wasted in the original processor (2p)?

e) When $t0 == $t1, how many instruction fetches are wasted in the original processor (2p)?

4. Modify the following single cycle MIPS datapath diagram to accommodate a new instruction `swai` (store word then auto-increment). The operation performs the regular `sw` operation, then post-increments the `rs` register by 1. Your modification may use simple adders, mux chips, wires, and new control signals. You may replace original labels where necessary. Recall the RTL for `sw` is:

`Mem[R[rs] + SignExt[imm16]] = R[rt]; PC=PC+4`, & that `sw` (and `swai`) has the following fields:

Opcode	Rs	Rt	Immediate

a) Modify the picture below and draw (or list) your changes below (you may draw or list on the exam paper or draw on the figure below). (7p)

b) We also wish to do the same thing with `lw`, namely create `lwai`. Will this work (please explain)? (3p)