S-87.3190 Computer Architecture (5 cr) Exam 23.5.2012

Please write clearly. Voit myös vastata suomeksi.

Mark your project completion year / Merkitse harjoitustyön suorittamisvuosi

A calculator is not allowed

1. a) Name two MIPS assembly instructions, which together can be used to create the effect of "branch on less than" (Note, just the instruction names). There are multiple answers, all of which will be accepted. Why isn't this instruction built in to MIPS assembly? (3p)
   b) Given the clock frequency and cycles per instruction (Ideal CPI) for two computers, can we predict which one would run a particular C program faster on the same input? Why (tell us how to do it) or why not (tell us all that is missing to be able to make a good prediction). (2p)
   c) Consider the three styles of I/O: 1) Polling, 2) DMA, 3) Interrupt Driven. Which provides the lowest latency? Which requires the fewest CPU cycles, and thus has the lowest impact on processor utilization? Please explain both very briefly. (3p)
   d) Explain briefly the major differences between a general purpose CPU (such as MIPS) and a DSP processor. (2p)

2. a) Explain the three MIPS instruction formats and explain the meaning of the instruction fields. (4p)
   b) For each of the following MIPS assembly language fragments on the right, decide which of the following applies (explain): (6p)
   a. Must stall
   b. Can avoid stalling by using forwarding
   c. Can execute without stalling or forwarding

1.
```
lw $t0, 0($t0)
addu $t1, $t0, $t0
```
2.
```
addu $t1, $t0, $t0
addiu $t2, $t0, 5
addiu $t4, $t1, 5
```
3.
```
addiu $t1, $t0, 1
addiu $t2, $t0, 2
addiu $t3, $t0, 3
addiu $t3, $t0, 4
addiu $t5, $t0, 5
```

3. a) Describe the operation of a set-associative cache. Compare it to other types of caches. (2p)
   b) Given a 2-way set-associative cache with LRU replacement policy, initially empty, and the following memory access pattern (all are byte addresses in decimal):
   8 0 4 32 36 8 0 4 16 0
   What is the hit rate, miss rate, and what blocks are in the cache after these accesses if the cache has 4 32-bit blocks? (4p)
   c) Consider a write-allocate, write-through, 4-way set-associative cache with 16 byte blocks and $64*2_{10}$ bytes of data bits. Assume a byte-addressed machine with 32-bit addresses. (4p)
   a. Partition the 32-bit address to index, offset, and tag. What is the size of each field in bits.
   b. Given the address DEADBEEFhex, what is the value of the index, offset, and tag? (Write your answers in hexadecimal.)
   c. How many cache management bits (bits in addition to the data) are there for each block? List them.

TURN OVER =>

4. a) Below is the single-cycle MIPS datapath presented during lecture. Your job is to modify the diagram for pipeline operation (3p)
   b) Also explain how the control changes with multi-cycle operation (2p)
   c) Explain how to stall the pipeline (use diagrams and/or text as necessary) (5p)